GX5961, GX5964

Digital I/O PXI Boards

User's Guide

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MARVIN TEST SOLUTIONS

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Table of Contents

Chapter 1 - Introduction

Manual Scope and Organization

Manual Scope

The purpose of this manual is to provide all the necessary information to install, use, and maintain the GX5961/GX5964 (referred in this manual as GX5960) digital subsystem. This manual assumes the reader has a general knowledge of PC based computers, Windows operating systems, and some understanding of digital I/O.

Refer to the GtDio6x for more information regarding the GtDio6x software including driver functions, programming examples, virtual panel and more.

Manual Organization

The **GX6961/4** manual is organized in the following manner:

Chapter	Content
Chapter 1 - Introduction	Introduces the this manual. Lists all the supported GX5960 boards and shows warning conventions used in the manual.
Chapter 2 – Overview	Describes the GX5960 series features, board description, architecture, specifications.
Chapter 3 –Installation and Connections	Provides instructions on how to install a GX5960 boards and the GtDio6x software.
Chapter 4 – Theory of Operation	Presents the theory of operation for the GX5960 boards, with an overview of operation and a simple description of operation for one channel (I/O pin).

Conventions Used in this Manual

Symbol Convention	Meaning
	Static Sensitive Electronic Devices. Handle Carefully.
	Warnings that may pose a personal danger to your health. For example, shock hazard.
	Cautions where computer components may be damaged if not handled carefully.
	Tips that aid you in your work.

Formatting Convention	Meaning
`Monospaced Text`	Examples of field syntax and programming samples.
Bold type	Words or characters you type as the manual instructs. For example: function or panel names.
Italic type	Specialized terms. Titles of other reference books. Placeholders for items you must supply, such as function parameters

Chapter 2 - Overview

Introduction

The GX5960 digital subsystem represents the highest level of performance available for PXI-based digital instrumentation. The GX5960 series includes two types of cards: GX5961 and GX5964. Based on the proven architecture of the Marvin Test Solutions PXI GX5055 and the EADS VXI T964 boards, the GX5960 series offers high performance pin electronics and a timing generator / sequencer in a compact, 6U PXI form factor. The GX5960 digital subsystem consists of one GX5961 Clock generator board with 16 driver / sensor channels and the GX5964 driver / sensor board, which supports 32 bi-directional I/O channels. Up to 528 digital I/O channels can be supported by the GX5960 digital subsystem. Each digital channel features a wide drive / sense voltage range of -15 V to +25V (maximum swing of 26 volts) which can be individually programmed for a drive hi, drive lo, sense hi, sense lo, and a load value (with commutation voltage level) – offering the user complete flexibility when creating test programs and fixtures for multiple types of UUTs. In addition, each channel offers a parametric measurement unit (PMU) for DC measurements.

Features

The GX5960 digital subsystem offers real-time digital stimulus, record, or expect data modes on all I/O channels and 32 high voltage utility I/O signals. Vector memory depth is 256K words. Each channel can be configured as an input or output on a per cycle basis. Six drive data formats are supported: NR, R1, R0, RZ, RC, and Complement Surround – providing flexibility to create a variety of bus cycles and waveforms to test board and box level products.

The GX5961 provides timing, input / output synchronization signals, and sequencing as well as 16 I/O channels. Additional channels can be added to the system by installing one or more, GX5964 boards which are interconnected via the PXI local and trigger busses. The GX5961 offers a flexible clock system which allows the module to operate as a timing master to the UUT or be slaved to the UUT's time base or some other external clock. All pin electronic resources are independent on a per channel basis – offering the user complete flexibility when programming drive / sense levels, source / sink currents, slew rate, skew, or PMU functions. The PMU can operate in the force voltage / measure current or force current / measure voltage mode and is useful for measuring a UUT's DC characteristics. In addition, each I/O channel includes an analog bus relay, which allows each channel to support hybrid channel (digital or analog) measurement capabilities. For analog stimulus / response measurements, the analog bus can be connected to external resources via a dedicated analog bus connector located on the front panel of the module.

The following provide a summary of the GX5960 series main features:

- Cycle based, 50 MHz dynamic digital subsystem with high performance timing generator
- High voltage pin electronics with per channel programmability
- Per channel parametric measurement unit (PMU)
- Analog bus access for each I/O channel
- Dual level drive / sense, and programmable load on a per channel basis
- 256 timing sets with 4 phases and 4 windows, alternate configurations include 1K and 4K timing sets
- 0 - 64 us phase and window programming range with 1ns resolution
- Supports up to 528 bi-directional I/O channels
- 256K of vector memory
- Comprehensive software tool set supports CASS legacy programs and importing of IEEE - 1445 compliant vector files
- 6U PXI Instrument

PXI Compatibility

The GX5960 subsystem can operate in any 6U PXI chassis that supports an air flow rate of 20 cfm/slot. Power for the pin electronics requires the use of external power supplies or the GX5960 subsystem can be used with a Marvin Test Solutions GX7005A / GX7015A PXI chassis which is designed specifically for high performance / high power digital applications and includes the necessary pin electronics power supplies as well as a high capacity cooling system.

Software

The GX5960 series is supplied with the GtDio6x software package that includes vector editing, a virtual instrument panel, and 32/64-bit DLL driver libraries and documentation. The virtual panel can be used to interactively program and control the instrument from a window that displays the instrument's current settings and status. In addition, interface files are provided to support access to programming tools and languages such as ATEasy, LabView, Microsoft® and Borland® C/C++, Microsoft Visual Basic®, Borland Delphi, and Pascal. On-Line help file and PDF User's Guide provides documentation that includes instructions for installing, using and programming the board.

Other optional software packages are available to support the importing of legacy digital test programs, CASS digital TPS'a or IEEE-1445 .tap files.

Refer to the GtDio6x for more information regarding the GtDio6x software including driver functions, programming examples, virtual panel and more.

Applications

The GX5960 digital subsystem can be used to support a variety of digital test applications including:

- Automatic Test Equipment (ATE)
- High-speed functional digital test
- Vector capture
- Hybrid and digital device test
- Memory testing
- LRU and SRU test

Boards Description

The GX5961 has 5 connectors on the front (Power, IO, Analog I/O, High Voltage and Auxiliary) and 3 PXI on the back.

Figure 2-1: GX5961 Board

The GX5964 has 3 connectors (Power, I/O and Analog I/O) on the front and 3 PXI on the back

Figure 2-2: GX5964 Board

GX5960 Models and Accessories

Model / Accessory	Description
GX5964, DIO board	Digital input/output and domain timing and control.
GX5961, Timing / Synch board	Timing and synchronization board. Includes 16 digital I/O channels, 4 aux I/O channels, 32 HV open collector channels
GT97110, DB9, sub D , 3’ female power connector cable	Supplies external power (Vcc &Vee) to the GX5964 and GX5961
GT95014, Connector Interface for the GX5960, SCSI to 100 Mil Grid, Single Ended	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
GT95015, Connector Interface for the GX5960, SCSI to 100 Mil Grid, Differential	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
GT95015- SCSI, Connector Interface for the GX5960, SCSI to 100 Mil Grid, Differential, no J2 connector installed	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
Connector I/F for GX5960, SCSI to 100 Mil Grid, Single Ended (both 64 & 14 pin)	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
GT95021, 2' shielded cable for GX5960 (68 Pin)	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
GT95022, 3' shielded cable for GX5960 (68 Pin)	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
GT95031, 6' shielded cable for GX5960 (68 Pin)	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
GT95028,10' shielded cable for GX5960 (68 Pin)	UUT I/O Interface, Analog Bus, Aux channels, HV I/O

GX5961/GX5954 Specifications

The following table outlines the specifications of the GX5961/GX5964 boards.

Timing

Internal Test Clock or System Clock (T0 Clock)	15.625 KHz to 50 MHz (using the 500 MHz master clock)
Test Clock Time base	Ext Reference Clock: 1 MHz to 80 MHz Internal reference clock: 20 MHz
T0_CLK Timing Resolution	1 ns (using the 500 MHz master clock)
Master Clock (Phase and Window Timing Source)	500 MHz (internal oscillator), +/- 50 ppm 40 MHz to 500 MHz (PLL), +/- 50 ppm
Master Clock Reference	Internal: 20 MHz PXI Clock 10 MHz Front panel: 5 MHz to 80 MHz
Timing Set Options	Index Mode: 256 Timing Set groups with 4 Phases, 4 Windows, and 4K sequence steps.
Phase Programming Range (Assert / Return)	0 ns to 64 us (using the 500 MHz master clock)
Window Programming Range (Open / Close)	0 ns to 64 us (using the 500 MHz master clock)
Phase and Window Timing Resolution	1 ns, using the 500 MHz master clock
Minimum Phase / Window Pulse Width; Assert / Return or Open / Close	8 ns, using the 500 MHz master clock
Phase / Window Reference	Phase: System or Vector Clock (selectable per Seq Step) Window: Vector clock only
Phase / Window Dead Time	10 ns at end of the Vector period (using 500 MHz master clock)
Clocks per vector	1 to 256 (selectable per Sequencer Step)
Pause / Vector Clutch	Phase and Window are frozen when Pause is asserted Pause on external event Pause based on phase edge Resume after programmed delay Resume on an external signal or CPU resume
Halt / System Clutch	Halt based on an external signal Halt on error Halt on a Sync pulse (used as a breakpoint)
Pause / Pattern and Halt / System Clutch Sources	PXI trigger lines Aux I/O 1-12 Ch. 1-32 (with mask/expect) , (GX5964) Ch. 1-16 (with mask / expect), (GX5961) Phase 1-4 (for Pause)

Drive / Sense Modes and Channel I/O

Note: All specifications based on pin electronic rails (VCC & VEE) of +18 V and -14 V) unless noted otherwise.

Number of I/O Channels	16 per card (GX5961) 32 per card (GX5964)
Analog bus	32 relay controlled connections to I/O pin (GX5964) 16 relay controlled connections to I/O pin (GX5961) Individual control for each channel
Test Modes	Dynamic or Static
Data Output Formats (per channel)	Drive Hi, Drive Lo, Hi-Z Formatted Data: No return, Return to 1, Return to 0, Return to Hi-Z, Return to complement, Surround by complement; selectable on a per channel basis
Drive Data Timing (per channel)	Data assert / de-assert based on Phases 1-4
Capture modes (per channel)	Mask Opening edge of Window Closing edge of Window Window – data is valid for entire window duration
Drive / expect mode	Output: Drive Hi, Drive Lo, Hi-Z Expect: 1, 0, OK, between states, or mask Keep last Toggle last Accumulate CRC-16
Recording modes (per sequence step)	Record errors for programmable inputs that have Good 1 & Good 0 Record errors for inputs that have only a Good 1 Record raw data based on NOT a Good 0 Record raw data based on a Good 1
Error address record	Record address for memory errors 1K deep error memory
Number of Drive and Sense Voltage References	GX5961: 16 Drive Hi / Drive Lo 16 Sense Hi / Sense Lo GX5964: 32 Drive Hi / Drive Lo 32 Sense Hi / Sense Lo
Drive Voltage Level (for specified Vee and Vcc voltages)	Drive Hi: -9 to +15V Drive Lo: -10 to + 11V
Drive High Range	Vee +5V to Vcc – 3

Drive Low Range	Vee +4V to Vcc – 7V
Maximum Drive Level Range	-14V to +26V
Drive Voltage Level Range	Min: 0.5 V p-p Max: 26 V p-p
Drive Voltage Accuracy	+/- 25 mv, < 26 V p-p drive voltage
Drive Voltage Resolution	16 bits
Output Impedance	12 or 50 ohms, typical
Drive Current	200 mA max per channel 1.6 A per board, max (GX5964) 0.8 A per board, max (GX5961)
Short Circuit Protection	Programmable current level with automatic disable, per channel basis
Slew Rate	0.1 to 1 V/ns, adjustable, programmable on a per channel basis
Channel Skew	320 ps, typical 500 ps max., after calibration, for all channels (Drive and sense)
Channel De-Skew	Range: +/- 5 ns Resolution: 312.5 ps - Programmable on a per channel basis. - Separate deskew control for drive and sense.
Sense Voltage Range	Sense Hi: -10 to +11 V Sense Lo: -10 to +11 V
Comparator range	Vee +2V to Vcc – 7V
Maximum Sense Level Range	-16V to +22V
Sense Voltage Threshold Accuracy	+/- 25 mv, < 26 V p-p sense voltage
Sense Voltage Resolution	16 bits
Input Leakage Current	50 nA, max
Pull-Up / Pull-Down Current Source/ Sink	+/ -24 ma, programmable on a per channel basis V commutate: -10 to +11 V., programmable on a per channel basis
Pull-Up / Pull-Down Current Source / Sink Accuracy	+/- 250 uA
Pull-Up / Pull-Down Current Source / Sink Resolution	16 bits

Vcom range	Vee +2V to Vcc – 7V
Voltage Commutation Accuracy	+/- 25mv, < 25 V range
Voltage Commutation Resolution	16 bits
Resistive Load	Range: Hi-Z, 250 ohm, 1 K ohm, programmable on a per channel basis
Memory	256K words

I/O Connections

Analog Bus (For Connections to Analog Instrumentation)	68 position SCSI III Type
I/O, External Control, Timing	68 position SCSI III Type
Vcc range	+10V to +29V
Vee range	-18V to -3V
Vcc - Vee range	+13V (min) to +32 V (max)
External Vcc / Vee	15 position D-sub, male +18 volts @ 6 A (GX5964) @3 A (GX5961) -14 volts @ 6 A (GX5964) @ 3 A (GX5961)

Analog Measurement Bus

Number Of Analog I/O Channels	16 per card (GX5961) 32 per card (GX5964)
Control	Independent connect / disconnect to each I/O channel, Independent disconnect relay to each digital channel
Switching Current	Maximum current: 0.5 A per channel
Operating Voltage	30 volts, max

Parametric Measurement Unit (PMU)

Number Of Parametric Measurement Units	32, one per channel (GX5964) 16, one per channel (GX5961)
Modes	Force voltage, measure current Force current, measure voltage
Force Voltage Range (for specified Vcc and Vee operating voltages)	-10 volts to + 15 volts
Maximum Force Voltage Range	Vee +4V to Vcc – 3V
Force Voltage Accuracy	+/- 25 mV, 25 volt range
Force Voltage & Current Resolution	16 bits
Force Current Range	+/- 30 mA FS +/- 200 mA FS
Force Current Accuracy	+/- 100 uA, 30 mA range +/- 8 mA, 200 mA range
Measure Voltage Range	-13 to +15 volts
Maximum Measure Voltage Range	Vee +1V to Vcc – 3V
Measure Voltage & Current Resolution	16 bits
Measure Voltage Accuracy	+/- 15 mV, -9 to +13 volt range
Measure Current Range	+/- 30 ma FS +/- 200 ma FS
Measure Current Accuracy	+/- 100 uA, (30 mA range) +/- 6 mA (200 mA range)

Environmental

Operating Temperature	0 to 50° C
Storage Temperature	-20° C to 70° C
Vibration	5 g at 500 Hz
Shock	10 g for 6 ms ½ sine

Physical Characteristics

Size	6U PXI , single slot
Weight	1.2 lbs (520 g)

Note: Specifications subject to change without notice.

GX5961 Timing / Sync Board Specifications

External Timing, Control & Status Signals

Sync outputs	2, Start of Sequence; Start of Sequence Step
General purpose aux I/O	12 channels 64 output selections for selected internal signals. 7 input selected signals
Input aux I/O selections	Synthesizer reference clock, System clock, Break (System Clutch), Halt (Vector Clutch), Sequence Jump signals
Output auxiliary I/O selections	Phase, Window, Waveform, Syncs, Seq flag, Seq Active, Seq Idle, T0_Clock , Pat_Clock, misc test signals.
Probe	Ground, Probe Button, Probe LED, Monitor
High Voltage I/O	Channels: 32 Output characteristics: Configuration: open collector Maximum output voltage: 28 VDC Maximum current: 1 A per byte Passive pull-up: 1 KOhm to 4.5 volts 0V shutdown: 28 VDC to 36 VDC Input characteristics: Threshold range: 0V to 10.235V Threshold resolution: 5 mV Threshold accuracy: +/- 35 mV + 1%

Note: Specifications subject to change without notice.

Chapter 3 - Installation and Connections

Getting Started

This section includes general hardware installation procedures for the GtDio6x board and installation instructions for the GtDio6x software. Before proceeding, please refer to the appropriate chapter to become familiar with the board being installed.

To Find Information on:	Refer to:
Hardware Installation	This Chapter
GtDio6x Driver Installation	This Chapter
Theory of Operation	Chapter 4

Interfaces and Accessories

The following accessories are available from Marvin Test Solutions the GX5960 series digital subsystem:

Part / Model Number	Description
GT97110, DB9, sub D , 3’ female power connector cable	Supplies external power (Vcc &Vee) to the GX5964 and GX5961
GT95014, Connector Interface for the GX5960, SCSI to 100 Mil Grid, Single Ended	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
GT95015, Connector Interface for the GX5960, SCSI to 100 Mil Grid, Differential	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
GT95015- SCSI, Connector Interface for the GX5960, SCSI to 100 Mil Grid, Differential, no J2 connector installed	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
Connector I/F for GX5055, SCSI to 100 Mil Grid, Single Ended (both 64 & 14 pin)	UUT I/O Interface, Analog Bus, Aux channels, HV I/O
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GT95028,10' shielded cable for GX5960 (68 Pin)	UUT I/O Interface, Analog Bus, Aux channels, HV I/O

Packing List

All GX5960 boards have the same basic packing list, which includes:

- GX5961, GX5964 Boards
- GtDio6x Software Disk

Unpacking and Inspection

After removing the board from the shipping carton:

 **Caution -** Static sensitive devices are present. Ground yourself to discharge static.

Remove the board from the static bag by handling only the metal portions.

Be sure to check the contents of the shipping carton to verify that all of the items found in it match the packing list.

Inspect the board for possible damage. If there is any sign of damage, return the board immediately. Please refer to the warranty information at the beginning of the manual.

System Requirements

The GX5960 PXI digital subsystem is designed to run on 6U PXI compatible chassis running under XP or newer (32/64 bit).

Each board in the digital subsystem requires one unoccupied 6U PXI bus slot.

Installation of the GtDio6X Software

Before installing the board it is recommended that you install the GtDio6x software as described in this section. To install the GtDio6x software, follow the instruction described below:

1. Insert the Marvin Test Solutions CD-ROM and locate the **GtDio6x.EXE** setup program. If you computer's Auto Run is configured, when inserting the CD a browser will show several options. Select the Marvin Test Solutions Files option and then locate the setup file. If Auto Run is not configured you can open the Windows explorer and locate the setup files (usually located under \Files\Setup folder). You can also check and see if a newer version of the software is available for download from Marvin Test Solutions' web site (www.marvintest.com), in that case download and use the newer version.

Run the GtDio6x setup and follow the instruction on the Setup screen to install the GtDio6x driver.

Note: When installing under Windows, you may be required to restart the setup after logging-in as a user with Administrator privileges. This is required in-order to upgrade your system with newer Windows components and to install kernel-mode device drivers (HW.SYS and HWDEVICE.SYS) which are required by the GtDio6x driver to access resources on your board.

The first setup screen to appear is the Welcome screen. Click **Next** to continue.

Enter the folder where GtDio6x is to be installed. Either click **Browse** to set up a new folder, or click **Next** to accept the default entry of `C:\Program Files\Marvin Test Solutions\GtDio6x` under 32-bit Windows or `C:\Program Files (x86)\Marvin Test Solutions\GtDio6x` under 64-bit Windows.

Select the type of Setup you wish and click **Next.** You can choose between **Typical**, **Run-Time** and **Custom** setups types. The **Typical** setup type installs all files. **Run-Time** setup type will install only the files required for controlling the board either from its driver or from its virtual panel. The **Custom** setup type lets you select from the available components.

The program will now start its installation. During the installation, Setup may upgrade some of the Windows shared components and files. The Setup may ask you to reboot after completion if some of the components it replaced were used by another application during the installation – do so before attempting to use the software.

You can now continue with the installation to install the board. After the board installation is complete you can test your installation by starting a panel program that lets you control the board interactively. The panel program can be started by selecting it from the Start, Programs, GtDio6x menu located in the Windows Taskbar.

Setup Maintenance Program

You can run the Setup again after GtDio6x has been installed from the original disk or from the Windows Control Panel – Add Remove Programs applet. Setup will be in the Maintenance mode when running for the second time. The Maintenance window show below allows you to modify the current GtDio6x installation. The following options are available in Maintenance mode:

- Modify. When you want to add or remove GtDio6x components.
- Repair. When you have corrupted files and need to reinstall.
- Remove. When you want to completely remove GtDio6x.

Select one of the options and click **Next** and follow the instruction on the screen until Setup is complete.

Overview of the GtDio6x Software

Once the software is installed, the following tools and software components are available:

- **GtDio6x Panel** – Configures and controls the GtDio6x board various features via an interactive user interface.
- **GtDio6x driver** - A DLL based function library (GTDIO6X.DLL for 32-bit applications or GTDIO6X64.DLL for 64-bit applications , located in the Windows System folder) used to program and control the board. The driver uses Marvin Test Solutions' HW driver or VISA supplied by third party vendor to access and control the GtDio6x boards.
- **Programming files and examples** – Interface files and libraries for support of various programming tools. A complete list of files and development tools supported by the driver is included in subsequent sections of this manual.
- **Documentation** – On-Line help and User's Guide for the board, GtDio6x driver and panel.
- **HW driver and PXI/PCI Explorer applet** – HW driver allows the GtDio6x driver to access and program the supported boards. The explorer applet configures the PXI chassis, controllers and devices. This is required for accurate identification of your PXI instruments later on when installed in your system. The applet configuration is saved to PXISYS.ini and PXIeSYS.ini and is used by Marvin Test Solutions instruments HW driver. The applet can be used to assign chassis numbers, Legacy Slot numbers and instrument alias names. The HW driver is installed and shared with all Marvin Test Solutions products to support accessing the PC resources. Similar to HW driver, provides a standard way for instrument manufacturers and users to write and use instruments drivers. VISA is a standard maintained by the VXI Plug & Play System Alliance and the PXI Systems Alliance organizations (http://www.vxipnp.org/, http://www.pxisa.org/). The VISA resource manager such as National Instruments **Measurement & Automation** (NI-MAX) displays and configures instruments and their address (similar to Marvin Test Solutions' PXI/PCI Explorer). The GtDio6x driver can work with either HW or VISA to control an access the supported boards.

Installation Folders

The GtDio6x driver files are installed in the default folder `C C:\Program Files\Marvin Test Solutions\GtDio6x` under 32-bit Windows or `C:\Program Files (x86)\Marvin Test Solutions\GtDio6x` under 64-bit Windows. During the installation, GtDio6x Setup creates and copies files to the following folders:

Name	Purpose / Contents
…\Marvin Test Solutions\GtDio6x	The GtDio6x folder. Contains panel programs, programming libraries, interface files and examples, on-line help files and other documentation.
…\Marvin Test Solutions\HW	HW device driver. Provide access to your board hardware resources such as memory, IO ports and PCI board configuration. See the README.TXT located in this directory for more information.
…\ATEasy\Drivers	ATEasy drivers folder. GtDio6x Driver and example are copied to this directory only if ATEasy is installed to your machine.
Windows System Folders	Contains the GtDio6x DLL and GtDio6x64.DLLdriver, HW driver shared files and some upgraded system components, such as the HTML help viewer, etc.

Configuring Your PXI System using the PXI/PCI Explorer

To configure your PXI/PCI system using the **PXI/PCI Explorer** applet follow these steps:

Start the PXI/PCI Explorer applet. The applet can be start from the Windows Control Panel or from the Windows Start Menu, **Marvin Test Solutions**, **HW**, **PXI/PCI Explorer**.

Identify Chassis and Controllers. After the PXI/PCI Explorer is started, it will scan your system for changes and will display the current configuration. The PXI/PCI Explorer automatically detects systems that have Marvin Test Solutions controllers and chassis. In addition, the applet detects PXI-MXI-3/4 extenders in your system (manufactured by National Instruments). If your chassis is not shown in the explorer main window, use the Identify Chassis/Controller commands to identify your system. Chassis and Controller manufacturers should provide INI and driver files for their chassis and controllers which are used by these commands.

Change chassis numbers, PXI devices Legacy Slot numbering and PXI devices Alias names. These are optional steps and can be performed if you would like your chassis to have different numbers. Legacy slots numbers are used by older Marvin Test Solutions driver. Alias names can provide a way to address a PXI device using a logical name (e.g. "FPGA1"). For more information regarding slot numbers and alias names, see the **GtDio6xInitialize** function.

Save your work. PXI Explorer saves the configuration to the following files located in the Windows folder: PXISYS.ini, PXIeSYS.ini and GxPxiSys.ini. Click on the **Save** button to save your changes. The PXI/Explorer will prompt you to save the changes if changes were made or detected (an asterisk sign ' *' in the caption indicated changes).

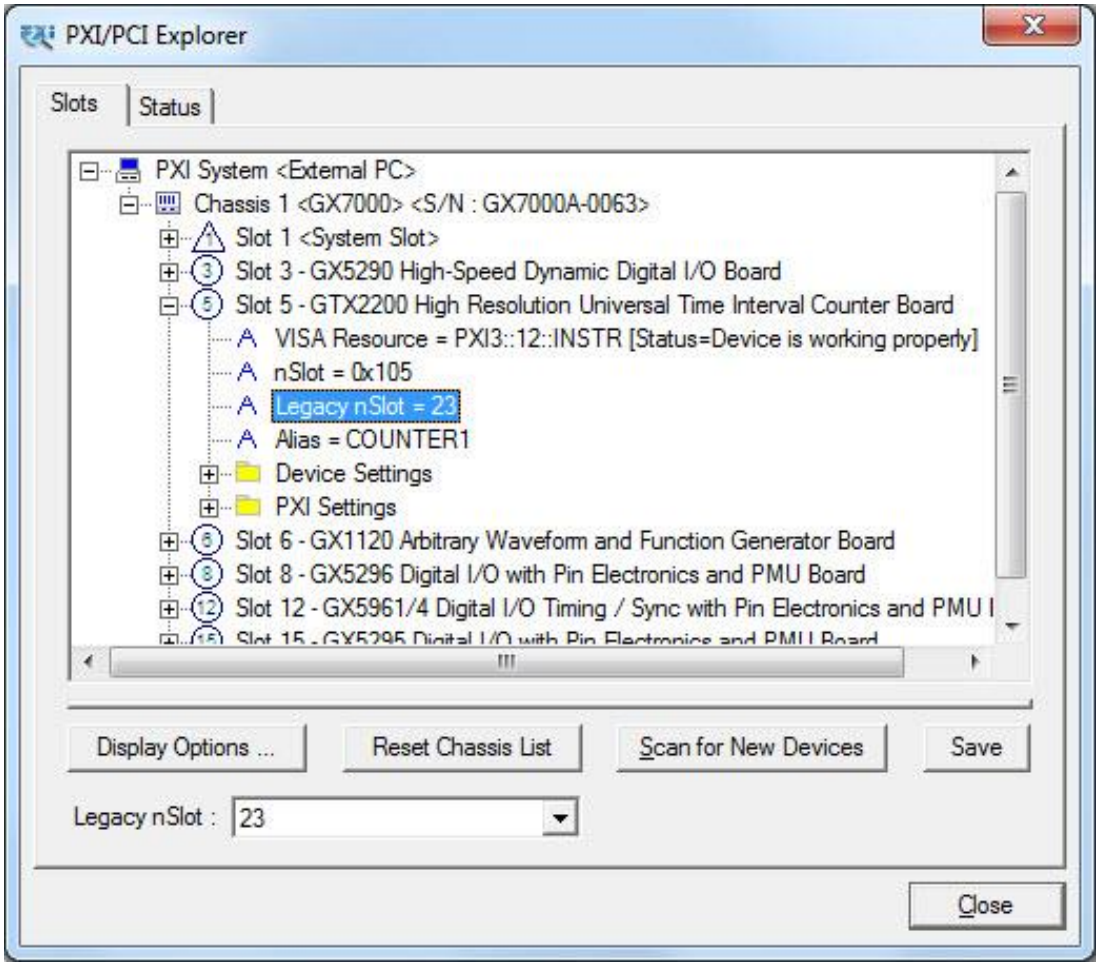


Figure 3-1: PXI/PCI Explorer

Board Installation

Before you Begin

- Install the GtDio6x driver as described in the prior section.
- Configure your PXI/PC system using **PXI/PCI Explorer** as described in the prior section.
- Verify that all the components listed in the packing list (see previous section in this chapter) are present.

Electric Static Discharge (ESD) Precautions

To reduce the risk of damage to the GX5960 board, the following precautions should be observed:

- Leave the board in the anti-static bags until installation requires removal. The anti-static bag protects the board from harmful static electricity.
- Save the anti-static bag in case the board is removed from the computer in the future.
- Carefully unpack and install the board. Do not drop or handle the board roughly.
- Handle the board by the edges. Avoid contact with any components on the circuit board.

Caution – Do not insert or remove any board while the computer is on. Turn off the power from the PXI chassis before installation.

Installing a Board

Install the board as follows:

1. Install the GtDio6x software as described in the next section.
2. Turn off the PXI chassis and unplug the power cord.
3. Locate a PXI empty slot on the PXI chassis.
4. Place the module edges into the PXI chassis rails (top and bottom).
5. Carefully slide the PXI board to the rear of the chassis, make sure that the ejector handles are pushed out (as shown in Figure 3-2).

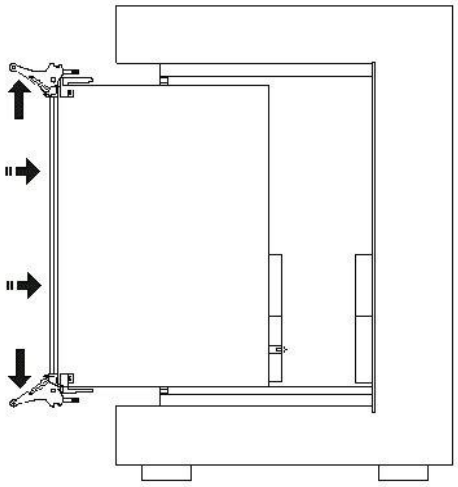


Figure 3-2: Ejector handle position during module insertion

After you feel resistance, push in the ejector handles as shown in Figure 3-3 to secure the module into the frame.

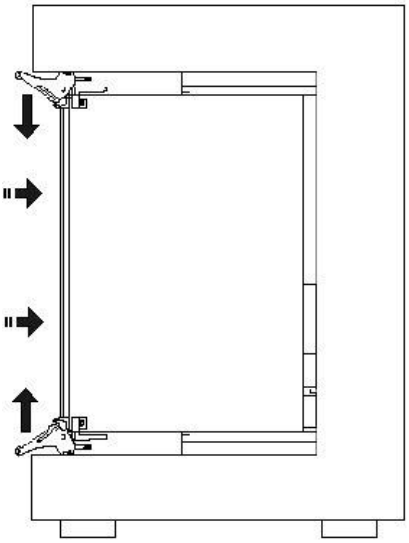


Figure 3-3: Ejector handle position after module insertion

Tighten the module's front panel to the chassis to secure the module in.

Connect any necessary cables to the board.

Plug the power cord in and turn on the PXI chassis.

Plug & Play Driver Installation

Plug & Play operating systems such as Windows 9x, Me, Windows 2000, XP, VISTA or Windows 7 (Not Windows NT) notifies the user that a new board was found using the **New Hardware Found** wizard after restarting the system with the new board.

If another Marvin Test Solutions board software package was already installed, Windows will suggest using the driver information file: HW.INF. The file is located in your Program Files\Marvin Test Solutions\HW folder. Click **Next** to confirm and follow the instructions on the screen to complete the driver installation.

If the operating system was unable to find the driver (since the GtDio6x driver was not installed prior to the board installation), you may install the GTDIO6X driver as described in the prior section, then click on the **Have Disk** button and browse to select the HW.INF file located in C:\Program File\Marvin Test Solutions\HW.

If you are unable to locate the driver click **Cancel** to the found New Hardware wizard and exit the New Hardware Found Wizard, install the GtDio6x driver, reboot your computer and repeat this procedure.

The Windows Device Manager (open from the System applet from the Windows Control Panel) must display the proper board name before continuing to use the board software (no Yellow warning icon shown next to device). If the device is displayed with an error you can select it and press delete and then press F5 to rescan the system again and to start the New Hardware Found wizard.

Removing a Board

Remove the board as follows:

1. Turn off the PXI chassis and unplug the power cord.
2. Locate a PXI slot on the PXI chassis.
3. Disconnect and remove any cables/connectors connected to the board.
4. Un-tighten the module's front panel screws to the chassis.
5. Push out the ejector handles and slide the PXI board away from the chassis.
6. Optionally – uninstall the GtDio6x driver.

Connectors and Jumpers

Figure 3-4 shows the available GX5964 and GX5961 board connectors:

GX5691 Connectors

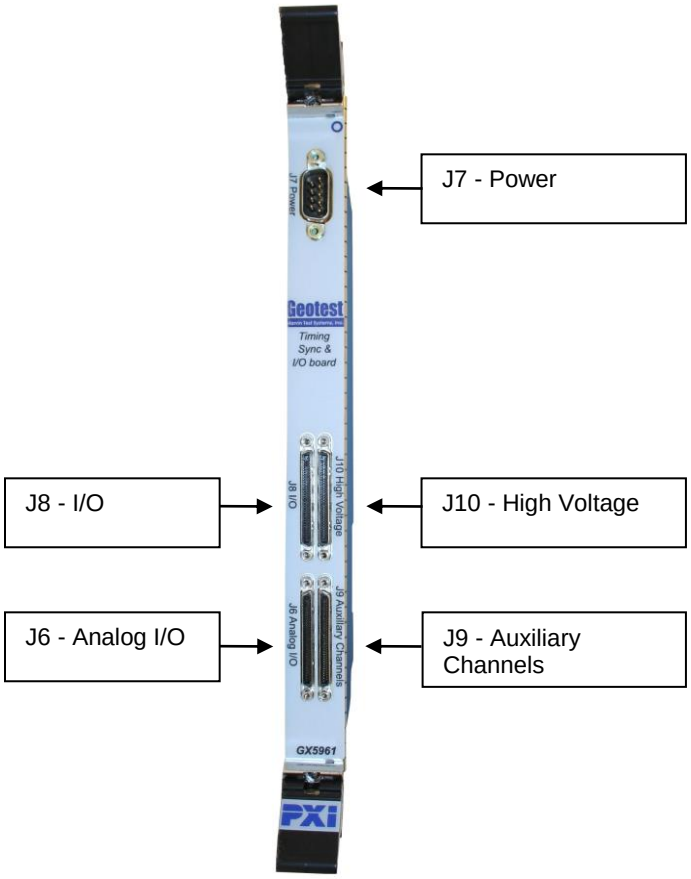


Figure 3-4: GX5961 Front Panel Connectors

The GX5961 has 4 connectors. All the connectors are available on the instrument's front panel. The GX5961 has the following connectors:

J7	Power - VCC and VEE power connections for pin electronics. Not used if the GX5961 is installed in a GX70x5A chassis.
J8	I/O - Programmable I/O Levels Data Connector Signals
J6	Analog I/O - 32 channel analog bus connections (connects to analog instrumentation / switch matrix)
J10	High Voltage - 32 high voltage (open collector) outputs / inputs
J9	Auxiliary Channels - External connections for clocking, external events and triggering

Table 3-1: GX5961 Connectors

GX5694 Connectors

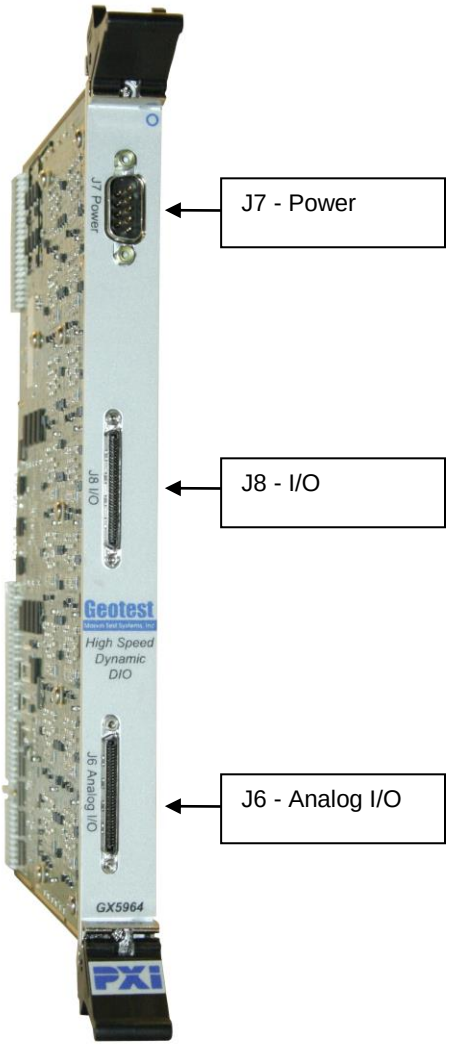


Figure 3-5: GX5964 Front Panel Connectors

The GX5964 has 3 connectors. All the connectors are available on the instrument's front panel. The GX5961 has the following connectors:

J7	Power - VCC and VEE power connections for pin electronics. Not used if the GX5961 is installed in a GX70x5A chassis.
J8	I/O - Programmable I/O Levels Data Connector Signals
J6	Analog I/O - 32 channel analog bus connections (connects to analog instrumentation / switch matrix).

Table 3-2: GX5964 Connectors

GX5961 J7- Front Panel Power Connector

The following table shows the power connector, J7, pin out. VCC supplied should be in the range of 10V to 29V, and VEE in the range of –3V to -20V.

Pin No.	Signal
1	ExtVCC
2	ExtVCC
3	ExtVEE
4	ExtVEE
5	Ext3.3V
6	GND
7	GND
8	GND
9	SHUTDOWN

Table 3-3: J7 – GX5961 Front Panel Power Connector Pinout

The following Figure shows a typical connection to the Power connector:

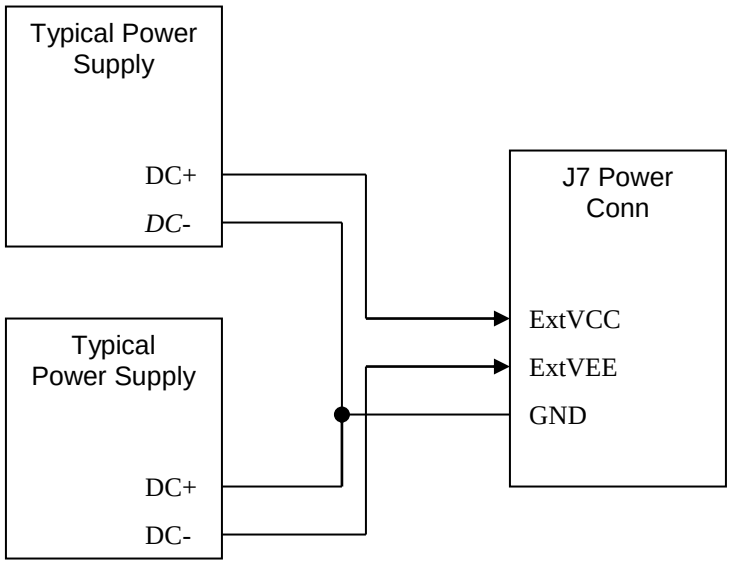


Figure 3-6: GX5961 Typical Power Connection Diagram

GX5961 J6- Front Panel Analog I/O Connector

Each of the Analog I/O channels has a relay for isolating the Pin Electronics from the DUT.

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	N/C	18	A_IO1	35	GND	52	GND
2	N/C	19	A_IO2	36	GND	53	GND
3	N/C	20	A_IO3	37	GND	54	GND
4	N/C	21	A_IO4	38	GND	55	GND
5	N/C	22	A_IO5	39	GND	56	GND
6	N/C	23	A_IO6	40	GND	57	GND
7	N/C	24	A_IO7	41	GND	58	GND
8	N/C	25	A_IO8	42	GND	59	GND
9	N/C	26	A_IO9	43	GND	60	GND
10	N/C	27	A_IO10	44	GND	61	GND
11	N/C	28	A_IO11	45	GND	62	GND
12	N/C	29	A_IO12	46	GND	63	GND
13	N/C	30	A_IO13	47	GND	64	GND
14	N/C	31	A_IO14	48	GND	65	GND
15	N/C	32	A_IO15	49	GND	66	GND
16	N/C	33	USER SCLK	50	GND	67	USER SDATA
17	A_IO0	34	USER SDATA VALID	51	GND	68	NC

Table 3-4: J6 – GX5961 Front Panel Analog I/O Connector Pinout

GX5961 J8- Front Panel I/O Connector

Each of the I/O channel has a relay for isolating the Pin Electronics from the DUT.

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	N/C	18	CH1	35	GND	52	GND
2	N/C	19	CH2	36	GND	53	GND
3	N/C	20	CH3	37	GND	54	GND
4	N/C	21	CH4	38	GND	55	GND
5	N/C	22	CH5	39	GND	56	GND
6	N/C	23	CH6	40	GND	57	GND
7	N/C	24	CH7	41	GND	58	GND
8	N/C	25	CH8	42	GND	59	GND
9	N/C	26	CH9	43	GND	60	GND
10	N/C	27	CH10	44	GND	61	GND
11	N/C	28	CH11	45	GND	62	GND
12	N/C	29	CH12	46	GND	63	GND
13	N/C	30	CH13	47	GND	64	GND
14	N/C	31	CH14	48	GND	65	GND
15	N/C	32	CH15	49	GND	66	GND
16	N/C	33	N/C	50	GND	67	N/C
17	CH0	34	EXFORCE VALID	51	GND	68	FP-DUTGND

Table 3-5: GX5961 J8 - Front Panel I/O Connector Pin out

GX5961 J9- Front Panel Auxiliary Channels Connector

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	AUX0	18	GND	35	GND	52	GND
2	AUX1	19	GND	36	GND	53	GND
3	AUX2	20	GND	37	GND	54	GND
4	AUX3	21	GND	38	GND	55	GND
5	AUX4	22	GND	39	GND	56	GND
6	AUX5	23	GND	40	GND	57	GND
7	AUX6	24	GND	41	GND	58	GND
8	AUX7	25	GND	42	GND	59	GND
9	AUX8 +	26	GND	43	AUX8 -	60	GND
10	AUX9 +	27	GND	44	AUX9 -	61	GND
11	AUX10 +	28	GND	45	AUX1 -	62	GND
12	AUX11 +	29	GND	46	AUX11 -	63	GND
13	GND	30	GND	47	PBUT	64	GND
14	GND	31	GND	48	PLED+B	65	GND
15	GND	32	GND	49	PCLK+B	66	GND
16	GND	33	GND	50	GND	67	GND
17	GND	34	GND	51	GND	68	GND

Table 3-6: GX5961 J9 - Front Panel Auxiliary Channels Connector Pinout

GX5961 J10- Front Panel High Voltage Connector

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	HV_PINS	18	HV_PINS	35	GND	52	GND
2	HV_PINS	19	HV_PINS	36	GND	53	GND
3	HV_PINS	20	HV_PINS	37	GND	54	GND
4	HV_PINS	21	HV_PINS	38	GND	55	GND
5	HV_PINS	22	HV_PINS	39	GND	56	GND
6	HV_PINS	23	HV_PINS	40	GND	57	GND
7	HV_PINS	24	HV_PINS	41	GND	58	GND
8	HV_PINS	25	HV_PINS	42	GND	59	GND
9	HV_PINS	26	HV_PINS	43	GND	60	GND
10	HV_PINS	27	HV_PINS	44	GND	61	GND
11	HV_PINS	28	HV_PINS	45	GND	62	GND
12	HV_PINS	29	HV_PINS	46	GND	63	GND
13	HV_PINS	30	HV_PINS	47	GND	64	GND
14	HV_PINS	31	HV_PINS	48	GND	65	GND
15	HV_PINS	32	HV_PINS	49	GND	66	GND
16	HV_PINS	33	HV_CLAMP_DIODE1	50	GND		
17	HV_PINS	34	HV_CLAMP_DIODE2	51	GND		

Table 3-7: GX5961 J10 - Front Panel High Voltage Connector Pinout

- HV_PINS: Open collector

GX5964 J7- Front Panel Power Connector

The following table shows the power connector, J7, pinout. VCC supplied should be in the range of 10V to 29V, and VEE in the range of –3V to -20V.

Pin No.	Signal
1	ExtVCC
2	ExtVCC
3	ExtVEE
4	ExtVEE
5	Ext3.3V
6	GND
7	GND
8	GND
9	SHUTDOWN

Table 3-8: J7 – GX5964 Front Panel Power Connector Pinout

The following Figure shows a typical connection to the Power connector:

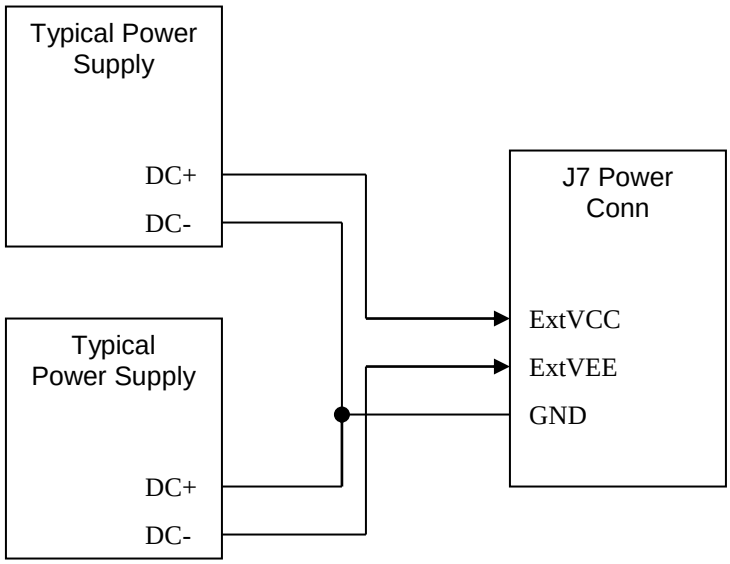


Figure 3-7: GX5964 Typical Power Connection Diagram

GX5964 J6- Front Panel Analog I/O Connector

Each of the Analog I/O channels has a relay for isolating the Pin Electronics from the DUT.

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	A_IO0	18	A_IO17	35	GND	52	GND
2	A_IO1	19	A_IO18	36	GND	53	GND
3	A_IO2	20	A_IO19	37	GND	54	GND
4	A_IO3	21	A_IO20	38	GND	55	GND
5	A_IO4	22	A_IO21	39	GND	56	GND
6	A_IO5	23	A_IO22	40	GND	57	GND
7	A_IO6	24	A_IO23	41	GND	58	GND
8	A_IO7	25	A_IO24	42	GND	59	GND
9	A_IO8	26	A_IO25	43	GND	60	GND
10	A_IO9	27	A_IO26	44	GND	61	GND
11	A_IO10	28	A_IO27	45	GND	62	GND
12	A_IO11	29	A_IO28	46	GND	63	GND
13	A_IO12	30	A_IO29	47	GND	64	GND
14	A_IO13	31	A_IO30	48	GND	65	GND
15	A_IO14	32	A_IO31	49	GND	66	GND
16	A_IO15	33	USER SCLK	50	GND	67	USER SDATA
17	A_IO16	34	USER SDATA VALID VALID	51	GND	68	NC

Table 3-9: GX5964 J6 - Front Panel Analog I/O Connector Pinout

GX5964 J8- Front Panel I/O Connector

Each of the I/O channel will has a relay for isolating the Pin Electronics from the DUT.

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	CH0	18	CH17	35	GND	52	GND
2	CH1	19	CH18	36	GND	53	GND
3	CH2	20	CH19	37	GND	54	GND
4	CH3	21	CH20	38	GND	55	GND
5	CH4	22	CH21	39	GND	56	GND
6	CH5	23	CH22	40	GND	57	GND
7	CH6	24	CH23	41	GND	58	GND
8	CH7	25	CH24	42	GND	59	GND
9	CH8	26	CH25	43	GND	60	GND
10	CH9	27	CH26	44	GND	61	GND
11	CH10	28	CH27	45	GND	62	GND
12	CH11	29	CH28	46	GND	63	GND
13	CH12	30	CH29	47	GND	64	GND
14	CH13	31	CH30	48	GND	65	GND
15	CH14	32	CH31	49	GND	66	GND
16	CH15	33	N/C	50	GND	67	N/C
17	CH16	34	EXFORCE VALID	51	GND	68	FP-DUTGND

Table 3-10: GX5964 J8- Front Panel I/O Connector

Chapter 4 - Theory of Operation

This chapter presents the theory of operation for the GX5960 boards. The following points are discussed:

- Overview
- Architecture
- Sequencer Engine
- Master, System and Vector Clocks
- Timing Sets, Timing Modes and Timing Set Value rules
- Vector Memory
- Step Memory
- Record Memory
- Error Address Memory
- Test Logic
- I/O Channels
- Probe

Overview

The GX5960 can run at frequencies up to 50 MHz with programmable timing sets applied on a per Step and Channel basis. Each board contains 32 (Gx5964) or 16 (Gx5961) I/O pins and each pin can be configured as an input or output on a per cycle basis. Each board has up to 4K Steps and 256K Vectors. A Vector represents the drive, expect, mask, and Tri-State data for one state (one Vector clock cycle). The Vector states are represented as ASCII characters.

A Step is a higher level that includes clock, timing, and control settings as well as a pointer into the Vector Memory. Different Steps can have overlapping Vector ranges (Vector Count and Offset). Each Step contains timing set information that will be applied to the relevant Vectors.

The Timing Set consists of a Drive Phase Assert, and Return edge as well as a Capture Window Open and Close edge. The Phase edges determine when a Vector state will be loaded within a clock cycle. The Window edges determine when the input will be sampled within a clock cycle. Consequently, each channel has an associated capture mode that allows the sequencer to capture input on the Window open edge, close edge, throughout the entire Window or not at all.

The GX5960 includes one unified (Vector) memory, for storing drive, expect, mask, and Tri-State data for each of the 256K Vectors. A separate Record memory is used to store up to 256K response states (raw logic HI and LO) or real time error states (depending on a Step's record mode) recorded during a sequencer run.

One of the GX5960's functional modules is the sequencer. The GX5960 sequencer functions as a state machine with five main states: RUN, SOFT PAUSE, HARD PAUSE, IDLE, and RESET. The sequencer runs each Step sequentially, applying timing (phase and window) settings to the Vectors associated with the Step. The sequencer will also perform a conditional jump, unconditional jump, subroutine jump, or loop if so instructed by a Step.

The sequencer has the ability to Handshake with various signals in order to synchronize with a UUT. Handshaking settings can be selected on a per Step basis where various Handshake Pause and Resume resources can be used. Handshake resources are configured for use by a Step. Configuring a Handshake resource entails selecting a source signal and test condition (high level, low level, rising edge, falling edge) to evaluate the source signal as a valid Pause or Resume condition.

Each digital pin can be individually programmed for a drive high, drive low, input threshold high, input threshold low, and a load value (with commutation voltage level) Slew rate is also adjustable, providing further flexibility when creating and verifying test programs and fixtures. Each channel output can be formatted programmatically to one of the following formats: No Return, Return to Off (HiZ), Return to Zero, Return to One, Return to Complement, Surround Complement, Force Zero, Force One, Force Off (HiZ), Force inverse Phase Output, Force Phase Output. Output formatting provides flexibility to create a variety of bus cycles and waveforms to test board and box level products. Each output channel can sense an over current sink or source condition, protecting each I/O channel from an overload condition. These conditions are recorded and the channel's output will go to a HI-Z state until the over current flag is cleared.

Each channel has its own Parametric Measurement Unit (PMU). The PMU offers the ability to perform analog measurements on each digital pin. Measurement configurations include force voltage, measure current and force current, measure voltage.

Additionally, under software control, each channel's operating temperature, Vcc / Vee voltage rails, drive high / drive low voltages, sense hi / sense lo voltages, and output current values can all be monitored and measured.

Each input channel's source and sink load currents can be set programmatically. The input channel current source forces the specified constant current to be active when the input voltage is above the high voltage clamp value. Each input channel's constant current voltage clamp can be set programmatically. With independent high and low clamping (commutating) voltages, the source and sink currents each have their own threshold voltage. Each input channel's load may be configured as a selectable resistor with pull-up and pull-down values or the value can be an open circuit. Each input channel's high and low voltage threshold comparator delays can be set programmatically. Each output channel has independent adjustments for the rising and falling edge slew rates. Additionally, each I/O channel can be programmed to have a skew delay. Each output channel's drive low and drive high voltages can be set programmatically. The total output driver voltage swing (output driver high voltage less output driver low voltage) is limited to 25V per channel.

Architecture

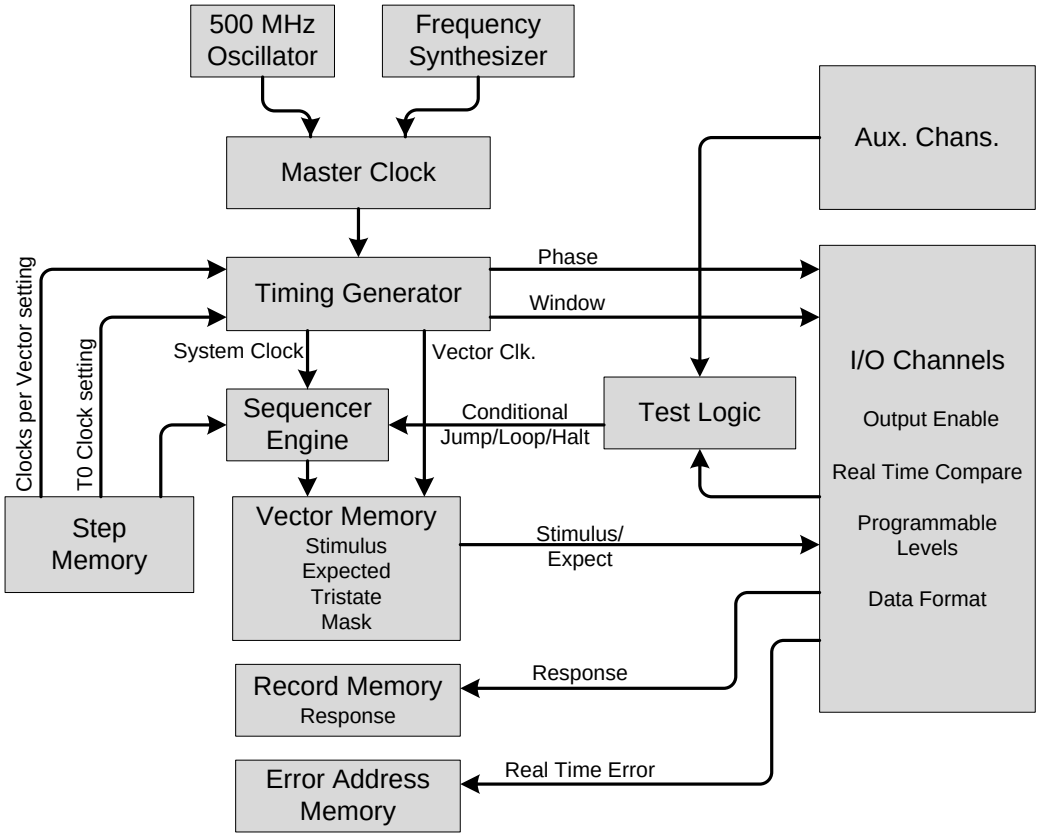


Figure 4-1: Architecture Block Diagram

Master Clock

The master clock functional block includes a fixed 500 MHz master clock oscillator and a Frequency Synthesizer which may be used instead of the 500 MHz oscillator. The reference clock for the Frequency Synthesizer can use the built-in 20 MHz oscillator, PXI Clock 10 MHz or an external oscillator in the range of 5 to 80 MHz

Timing Generator

Using the Master Clock as a basis, the Timing Generator block produces a, Phase, Window, Vector and System clock signals. In a Master/Slave configuration, these signals are broadcast across the PXI Backplane (B/P) on the Local Bus signal lines to other board sequencers. The System clock is used by the sequencer to start each phase and window along with incrementing the Vector and Record memories. The System clock can be sourced from the internal T0 clock or an external source connected to an auxiliary channel.

Step Memory and Sequencer Engine

The Step Memory defines the order in which Vectors will be driven or sensed (recorded). This block provides the addressing to the Vector Memory and the Record Memory. The Step Memory also contains the T0 Clock period, Phase, Window, CPV (clocks per vector) and a Control statement for conditional jumping and looping

Vector Memory

The stimulus, expect, and Tri-State data for each vector and channel is stored in the Vector Memory.

Record Memory

The Record Memory stores individual channel error results or raw response data depending on the current Step's record mode.

Test Logic

The test logic monitors Auxiliary Channels, Error signal, Channel Test signals, and PXI triggers and provides the Sequencer Engine with input for its conditional logic.

Aux I/O

The auxiliary I/O block offers a range of useful user and diagnostic input and output signals for user applications. The inputs may be used for synchronizing or triggering the GX5960 with UUT generated events. Note that the Aux I/O functions are only present on the GX5961 board.

I/O Channels

The channel I/O block takes the Stimulus data, applies the data format and outputs the formatted data according to the phase timing. The resultant Drive and Enable signals go to the Channel Drivers (pin electronics).

The Response High and Response Low signals from the Receivers are examined and based on the window timing and capture mode and the response is analyzed with respect to the Expect data. The cumulative Error signal goes to the Test Logic block so it can be used for Jumping, Halting and Counting of Errors.

Sequencer

The GX5960 board has six basic operational states: **Reset, Idle, Standby, Soft Pause, Hard Pause** and **Run**. **Error! Reference source not found.** is a block diagram showing the relationship of these operational states.

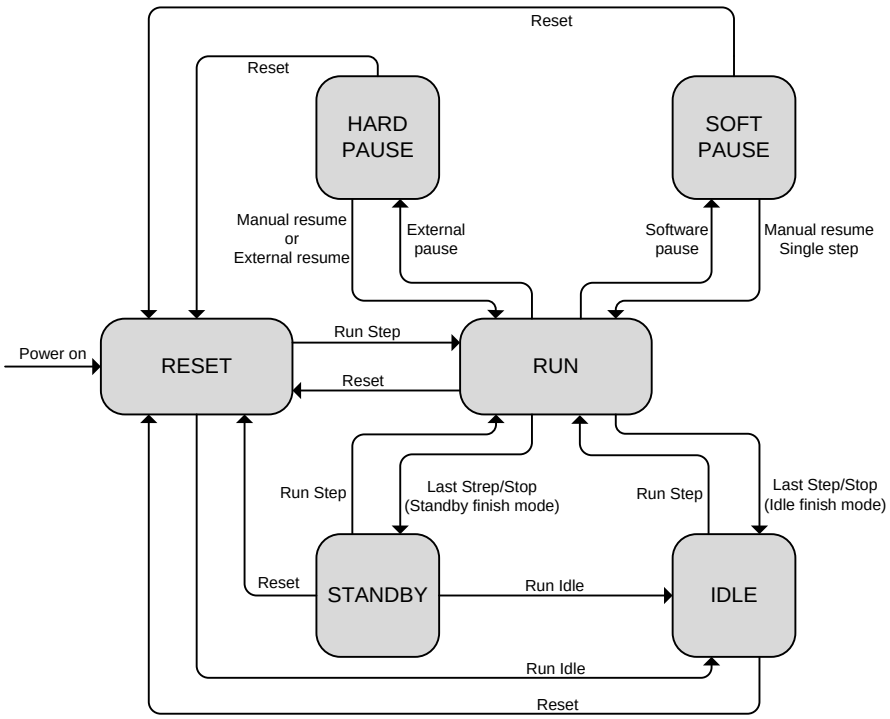


Figure 4-2: GX5960 Operational States

Reset State

When the sequencer is first powered, or goes through a **Reset** or **Sequencer Reset**, it is in the Reset State. In this state the sequencer is continuously looping on the first vector assigned to Step 0. All real-time compare errors are cleared and the sequencer is ready to enter another state.

Idle State

The sequencer will continuously run through all Vectors assigned to the Idle Step. During this time, the Vector Memory is busy and cannot be accessed by the User. The Idle state can be entered when a Run ends or is stopped manually by the user. It can also be entered manually by the user, before entering the Run State.

Standby State

The sequencer will run only the first Vector of the selected Finish Step. The Standby State is entered when a Run ends or is stopped manually by the user. The Standby State allows the user to maintain UUT stimulation between Digital Bursts.

Run State

The Run State is the primary execution state. The Run State can be entered manually, by user command or through an external trigger. The sequencer will run through each Step and execute each Vector assigned to the respective Step. The Vector Memory is busy during this state and it cannot be accessed by the User.

Soft Pause State

The Soft Pause State is entered through manual intervention by the user. The different Software Pause modes can be set by the user to allow different behaviors to occur when a Software Pause is commanded by the user. During the Paused state, the last Vector is output statically on the I/O channels.

Hard Pause State

The Hard Pause State is entered through external triggering or handshaking signals. The Hard Pause State is similar to the Soft Pause State and is controlled by the current Pause Mode.

Finish/Idle State

One of the unique features of the GX5960 is the Finish/Idle state. After the execution of a burst, the sequencer will enter the Idle/Standby state. The user can define the Finish/idle state timing and vector such that UUT stimulus can be maintained between vector bursts. A single vector can be specified so that the vector memory can be updated (Finish) or a group of vectors can be specified (Idle) during this state.

The user can disable the timing set phases/windows during the Finish/Idle state by setting Assert/Return and Open/Close values to zero. See **GtDio6xSequencerSetFinishStep** in the Functions Reference chapter for information.

Clocks

The Gx5960 system uses several clocking signals to generate and capture digital vectors from the I/O Channels.

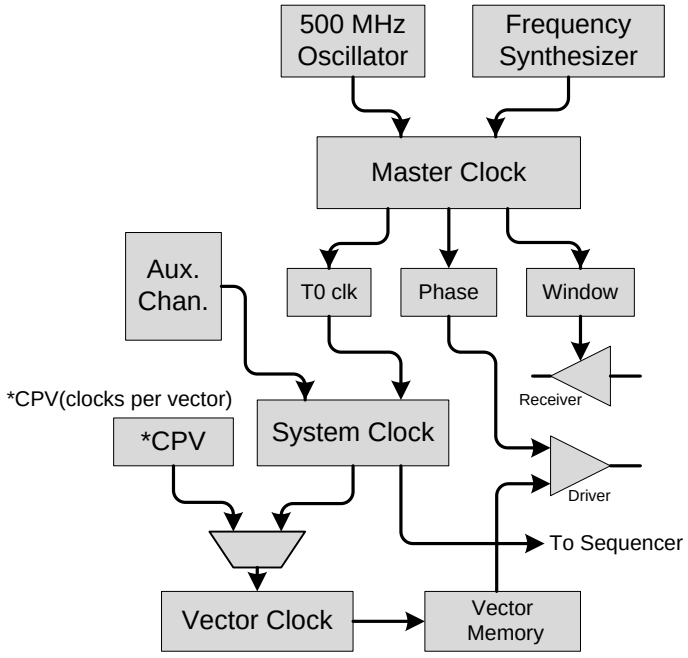


Figure 4-3: Clock Architecture Overview

Master Clock

The master clock defines the edge or timing resolution. This block contains a fixed 500 MHz master clock oscillator and a Frequency Synthesizer (FS) which may be used in lieu of the 500 MHz oscillator. The reference clock for the Frequency Synthesizer may be the built-in 20 MHz oscillator, 10 MHz PXI clock or an external oscillator in the range of 5 to 80 MHz.

Source	Description
500 MHz	Sequencer (timing) resolution set to 1ns
Frequency Synthesizer	Sequencer resolution set to 1 / (2 * FS) For example, if FS = 100 MHz Resolution = 1 / (2 * 100,000,000) Resolution = 5ns

Table 4-4: Master Clock Source Settings

See **GtDio6xSequencerSetMasterClockSource** in the functions reference chapter for information.

System Clock

The System Clock is used to apply Step settings (such as Phase, Window, and T0 Clock) to the sequencer. The System Clock also generates the Vector Clock which is used to define a Vector's period.

Source	Description
Internal T0 Clock	System Clock driven by the internal T0 Clock which is programmed per Step.
AUX0-AUX11	System Clock driven by the external auxiliary channels.
Frequency Synthesizer	System Clock driven by the internal frequency synthesizer signal.

Table 4-5: System Clock Source Settings

The relevant API function is: **GtDio6xSequencerSetSystemClockSource**

Vector Clock

The Vector Clock is derived from the System Clock and the Clocks per Vector setting. The Vector Clock period will equal the System Clock Period divided by the Clocks per Vector setting. The Vector Clock is used to clock out Vectors from memory when the Sequencer is running.

See **GtDio6xStepSetClock** in the functions reference chapter for information.

Timing Sets

The GX5960 Timing Subsystem is comprised of the System Clock, the Vector Clock and a Timing Generator which generates the Phase Assert, Phase Return, Window Open, and Window Close signals. The System Clock Cycle determines the base frequency at which Vectors are assigned to the currently running Step which will be clocked from the Vector Memory. The Vector Clock is derived from the System Clock, and is controlled by the Clocks per Vector setting. The Vector Clock period is equal to the System Clock period multiplied by the Clocks per Vector. The Phase and Window signals determine how and when (in conjunction with the Data Format) a Vector's output state will be applied to the I/O Pins within a System /Vector Clock cycle. The Phase Reset Source setting determines which clock (System or Vector) will cause the Phase signal to reset and begin again.

A timing set consists of one Phase and Window; there can be one or four timing sets per group. The timing sets are used to control the channel drivers and receivers.

Phase

A Phase controls the driver output operation and consists of an Assert and a Return edge. The Assert signal loads the current pattern code in to the output driver. The Return signal is used to enable the format code in the driver. The Return signal is not used for the Non Return format code.

Window

The Window controls the signal capture for the receiver and consists of an Open and Close edge. Each channel can be set to one of three capture modes. In Windowed mode, the Window Open signal begins signal capture and the Window Close ends the capture. In Open Edge mode, the Window Open edge strobes the channel comparator input and the Close Edge is ignored. In Close Edge mode, the Window Close edge strobes the channel comparator input and the Open Edge is ignored.

The Phase timing logic can be triggered by either the System Clock or the Vector Clock. The Window timing logic is triggered by the Vector Clock.

A timing diagram of the System Clock, Vector Clock, Window, and Phase signals is shown in Figure 4-4.

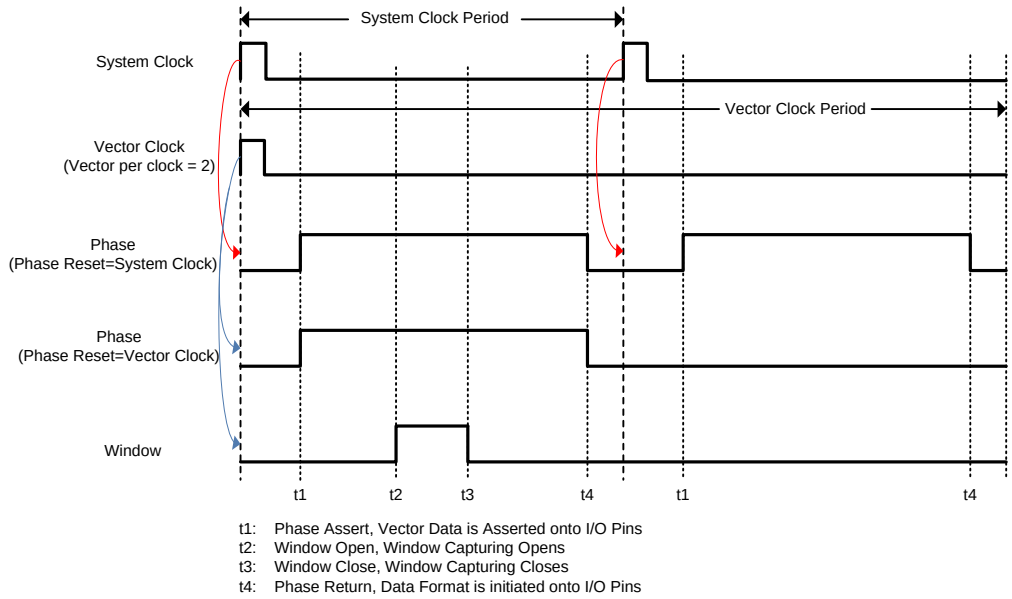


Figure 4-6: System Clock, Vector Clock, Phase and Window Timing Diagram

Indexed Timing Mode

Timing Sets are used in Indexed Timing Sets mode which consists of 4096 Steps, each Step can be programmed to point to any of the 256 timing set located in the Timing Set Index Memory. Each timing set is composed of four pairs of Phase and Window settings as follows:

Timing Set Index Number	TSet 0: First pair of Phase and Window in the specified Timing Set Memory Index	Phase Assert 0 Phase Return 0 Window Open 0 WindowClose 0
	TSet 1: Second pair of Phase and Window in the specified Timing Set Memory Index	Phase Assert 1 Phase Return 1 Window Open 1 WindowClose 1
	TSet 2: Third pair of Phase and Window in the specified Timing Set Memory Index	Phase Assert 2 Phase Return 2 Window Open 2 WindowClose 2
	TSet 3: Fourth pair of Phase and Window in the specified Timing Set Memory Index	Phase Assert 3 Phase Return 3 Window Open 3 WindowClose 3

Table 4-7: Componenets of a single Timing Set

The user can assign one of the four timing set's Index number to any I/O channel or a range I/O channels. The Timing Set to I/O channel assignment relationship will be maintained and applied to every Step / Timing Set in Step Memory. Timing set index is programmed per Step. Each channel can be set to use any of the four Phase Assert and Phase Return pair, as well any of the Window Open and WindowClose pairs. E.g. Channel 1 can have TSet 0 for Phase Assert and Phase Return, and TSet 2 as the Window Open and WindowClose. Each step can be assign one of the 256 Timing Set Index numbers, while the channels will maintain the Phase and Window TSwt settings.

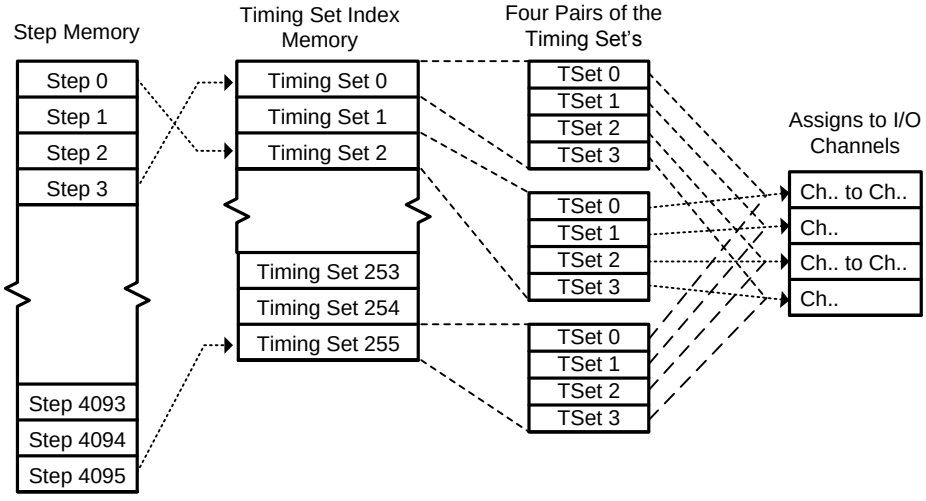


Figure 4-8: Indexed Timing Sets Diagram

Note: that only one Timing Set mode can be used for all the Steps in Vector memory.

Timing Set RulesFor valid timing set signal operation, the following timing rules must be followed (in the following descriptions a Master Clock refers to the selected (500 MHz or Frequency Synthesizer) master clock source):

- Phase pulse width must be greater than 3.5 clocks, i.e., the Return value must be at least 4 clocks more than the Assert value.
- Window pulse width must be greater than 3.5 clocks, i.e., the Close value must be at least 4 clocks more than the Open value.

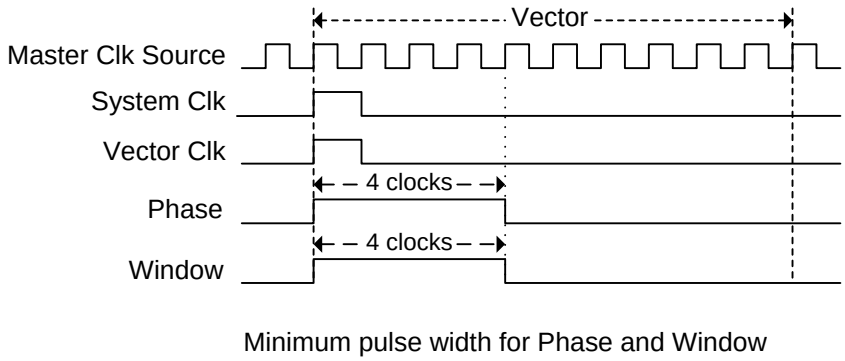


Figure 4-9: Timing Set Rules

- End of Vector period Dead Time. Phase Return, Window Close and Window Open edges must occur before the end of the Vector period to allow for Domain Error propagation delay. During this delay errors are not recorded or processed, this delay is referred to as Dead Time; this occurs when the Error Count memory and Error Address memory are updated or a Halt on Error pause is enabled. The Phase return edge has a minimum of 8ns of Dead Time regardless of the number of boards comprising a domain. The Window capture edge (Open, Close or Windowed) Dead Time is dependent on the number of boards that comprise a domain. The Dead Time range for various board configurations is as follows:

Number of Boards	Dead Time (Error Count, Error Address)	Dead Time (Halt on Error)
1	11ns	38ns + (RO x 2)
2	24ns	56ns + (RO x 2)
3	26ns	57ns + (RO x 2)
4	27ns	58ns + (RO x 2)
5	28ns	59ns + (RO x 2)
6	29ns	60ns + (RO x 2)

RO = Record Offset

Table 4-10: Dead Times

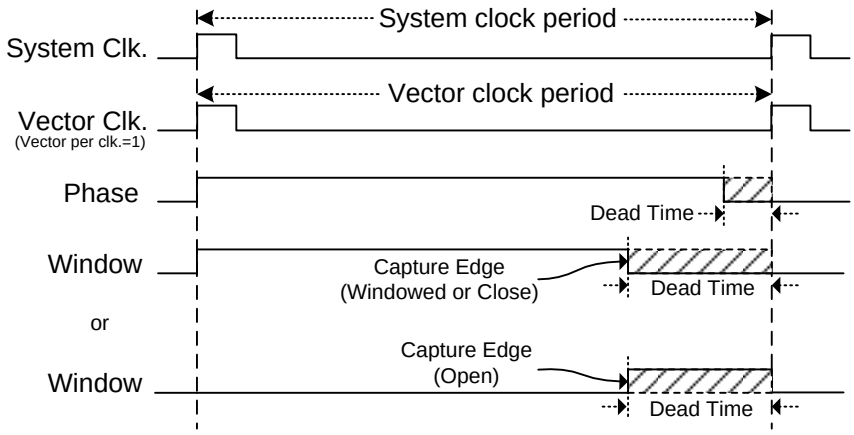


Figure 4-11: Phase and Window Dead Time Diagram

Phases and Windows are allowed to extend past the initial pattern period if multiple clocks per vector (CPV > 1) are programmed.

Vector Memory

The Gx5960 has a unified Vector memory which combines several pieces of information. Each Vector channel state is represented in the form of an ASCII character. The ASCII Character encodes the Output, Real Time Expect, Tristate Control (Direction), and Mask information for a particular channel within a Vector. The Vector Memory API functions allow the user to write and read from Vector Memory to any desired channel or group of channels for a given range of Vectors.

A separate Record Memory contains either response data or error data depending on the Record Mode selected for a particular Step. If the Step's Record Mode is set to Response, a '1' indicates a logic high response, and a '0' indicates a logic low response. If the Step's Record Mode is set to Error, a '1' indicates a real time compare error, and a '0' means no real time compare error occurred. The Record Memory stores up to 256K of response vectors. The indices of the Record Memory are mapped 1 to 1 with the Vector Memory.

Opcode	Description	Driver State	Drive Level	Comparator Expect	Invert Code
1	Drive High, Don't Expect (Don't Care)	On	VoH	None	Drive Low '0'
0	Drive Low, Don't Expect (Don't Care)	On	VoL	None	Drive High '1'
h	Drive High, Expect High	On	VoH	>ViH	Drive Low, Expect Low 'l'
l	Drive Low, Expect Low	On	VoL	<ViL	Drive High, Expect High 'h'
H	Expect High, Don't Drive	Off	X	>ViH	Expect Valid Low 'L'
L	Expect Low, Don't Drive	Off	X	<ViL	Expect Valid High 'H'
Z	Tristate (Disabled)	Off	N/A	None	Disable Channel 'Z'
/	Drive Low, Expect High	On	VoL	>ViH	Drive High, Expect Low '\'
****	Drive High, Expect Low	On	VoH	<ViL	Drive Low, Expect High '/'
V	Expect Valid Level	Off	X	>ViH OR <ViL	Expect Invalid 'B'
B	Expect Invalid Level	Off	X	<ViH AND >ViL	Expect Valid 'V'
R	Repeat previous opcode	Repeats the last non repeat/invert code.			
I	Invert previous opcode	Inverts the last non repeat/invert code. Refer to Invert Code			
C	Collect CRC	Off	X	None	Collect CRC 'C'

Table 4-12: Vector Opcode Description Sequencer Step Memory

When running the Sequencer executes a series of one or more Steps, as defined by the user. This execution is known as a Burst. The Burst will continue until a non-jumping Step is executed with the Last Step flag set to True. At this point, the Sequencer will enter the Finish or Idle Step (see Finish/Idle State) A Step points to a block of vectors (contiguous, in vector memory) and applies timing, control, and record parameters during run-time.

Vector Assignment

Each Step can be assigned a block of vectors from the vector memory. The Step contains the number of vectors and the start offset (from Vector memory 0) address. Steps can have overlapping or identical vector assignments (offset location and number of Vectors). Note that the vector offset must be a multiple of 4.

See **GtDio6xStepSetVectorCount** in the functions reference chapter for more information.

T0 Clock

Each Step contains a programmable value for the Vector Clock period (T0 Clock). The Vector Clock period is programmed in terms of ½ of the selected (Master Clock or Frequency Synthesizer) clock period. When using the default 500 MHz onboard Master Clock, the resolution is 1nS.

When the System Clock source is set to the internal T0 CLK, the System Clock period setting is the programmed ½ the Master Clock period.

For example if the Master Clock is set to 500 MHz, then a setting of 20 would be

20 * (1/2 (2ns)) = 20ns.

With a Master Clock of 100 MHz edge resolution would be;

20 * (1/2 (10ns)) = 100ns.

The valid setting values for T0 CLK are from 20 to 65550 and must be a multiple of two.

See **GtDio6xStepSetClock** in the functions reference chapter for more information.

Timing

Each Step contains Timing Set information which defines the Phase Assert/Return, and Window Open/Close edges. This setting is in terms of ½ Master Clock cycles. When using the default 500 MHz onboard Master Clock, the resolution is 1nS.

The number of Timing Sets available per Step, and the way to configure them (Multi, Single or Indexed mode) is described in the **Timing Mode** section of this chapter.

See **GtDio6xStepSetTimingSets, GtDio6xStepSetTimingSetIndex** for more information.

Clocks per Vector

Two clocks are available for triggering the phase's and window's timing, System Clock and Vector Clock.

The Clocks per Vector determines the number of System Clocks that will be generated for each Vector Clock. When Clocks per Vector = 1, the Vector Clock period is equal to System Clock period. When Clocks per Vector = 2, the Vector Clock period is two times the System Clock period.

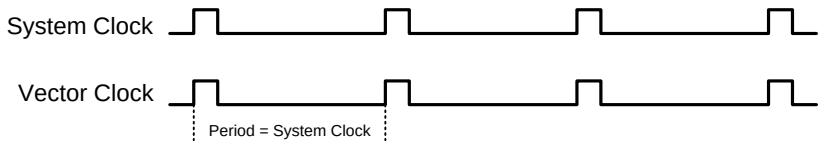


Figure 4-13: Timing Diagram of Clocks per Vector at 1

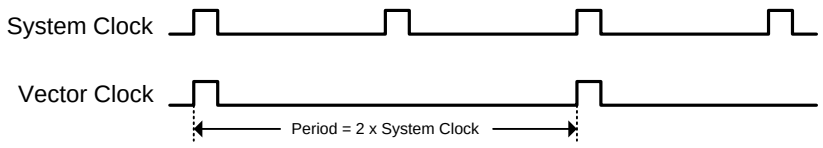


Figure 4-14: Timing Diagram of Clocks per Vector at 2

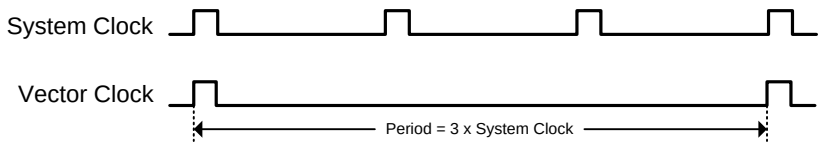


Figure 4-15: Timing Diagram of Clocks per Vector at 3

See **GtDio6xStepSetClock** for more information.

Record Mode

Each Step can be configured to use the Record Memory in a specific manner.

The Step can be configured to record a response or perform a real time compare of error states.

The user can also choose to not write to the record memory. The following describes the various record modes:

- None - All three record memories are disabled.
- Record Count - The Error Count and Error Address Memory are enabled.
- Record Error - All three memories are enabled and the Record Memory is set to record error data.
- Record Response - All three memories are enabled and the Record Memory is set to record response data.

See **GtDio6xStepSetRecordMode** for more information.

Phase Reset Source

The phase reset source allows the user to select the phase reset signal source which can be the System Clock or the Vector Clock. The phase reset signal restarts the phase assert and return timing.

See **GtDio6xStepSetPhaseTriggerSource** for more information.

Last Step Flag

This flag indicates whether the current step is the last step of the sequence burst or a sub-step of a multi step burst.

See **GtDio6xStepSetLast** for more information.

Control Logic

There is one control statement that is evaluated at the end of each Step by the Sequencer. The control statement is part of the Step's memory structure. At the end of a Step (where one or more Vectors were executed), a control statement allows the Sequencer to Jump, Go to Subroutine, Loop, Stop, or Continue to the next Step. The branching can be made on the following conditions:

- Always – Always evaluate the conditional statement as True
- Not Pass – Conditional statement is True if the Step has not Passed
- Not Fail – Conditional statement is True if the Step has not Failed
- Fail – Conditional statement is True if the Step has failed
- Pass – Conditional statement is True if the Step has passed
- Burst Fail – Conditional statement is True if the Burst failed
- Burst Pass – Conditional statement is True if the Burst passed
- Control Resource 0 – Conditional statement is True if Control Resource 0 is True
- Not Control Resource 0 – Conditional statement is True if the Control Resource is Not True
- Control Resource 1 – Conditional statement is True if the Control Resource 1 is True

- Not Control Resource 1 – Conditional statement is True if the Control Resource 1 is Not True
- Control Resource 2 – Conditional statement is True if the Control Resource 2 is True
- Not Control Resource 2 – Conditional statement is True if the Control Resource 2 is Not True
- Control Resource 3 – Conditional statement is True if the Control Resource 3 is True
- Not Control Resource 3 – Conditional statement is True if the Control Resource 3 is Not True

See **GtDio6xStepSetControl** for more information.

Record Memory

A separate Record Memory contains either response data or error data depending on the Record Mode selected for a particular Step. If the Step's Record Mode is set to Response, a '1' indicates a logic high response, and a '0' indicates a logic low response. If the Step's Record Mode is set to Error, a '1' indicates a real time compare error, and a '0' means no real time compare error occurred. The Record Memory can store up to 256K response vectors. The indices of the Record Memory are mapped 1 to 1 with the Vector Memory.

Test Logic

The Test Logic circuit consists of Control Resources and Triggers which are used to provide the sequencer with testable conditions by which a certain action can be taken.

Control Resource

A Control Resource is a user configurable signal which is tested in the Test Logic block; the results of the test are used by the Sequencer during the execution of the control statement at the end of each Step. There are four selectable Control Resources (0, 1, 2, 3); the following input signal sources can be assigned to any one of the four Control Resources:

- Aux Channels 0 to 11
- Channel Test 0
- PXI Trigger 0 to 7.

The Control Resource tests the assigned input signal (the source signal can also be inverted before testing) for one of the following actions:

- Low Level.
- High Level.
- Rising Edge.
- Falling Edge.

The generated Control Resource signal is used in the Step's control statement as a conditional Boolean to determine if a Jump or Loop should occur.

There is a Reset Mode that controls how and when the Control Resource signal is reset to a low:

- Reset at the start of a Burst.
- Reset at the start of a Step.
- Reset at the start of a Step and when resuming a paused Sequencer.

See **GtDio6xTrigConfigSetJumpTrigger** for more information.

Triggers

A Trigger is a user configurable signal which is tested in the Test Logic block; the results of the test are used by the Sequencer during execution to perform an action such as Run, Stop, or Pause. There are three Trigger available:

- Run Trigger
- Stop Trigger
- Pause Trigger

There are several selectable Trigger sources; these source signals can be inverted before being tested. The following input signal sources can be assigned to be a Trigger signal:

- Aux Channels 0 to 11
- Channel Test 0
- PXI Trigger 0 to 7.

Once the Trigger source is selected, the Trigger signal can be tested in one of the following ways:

- Low Level
- High Level
- Rising Edge
- Falling Edge

There is a Reset Mode that controls how and when the Trigger Resource signal is reset to low:

- Reset at the start of a Burst.
- Reset at the start of a Step.

See GtDio6xSetTrigger for more information.

Channel Test

There are 4 Channel Test signals (Channel Test 0 to Channel Test 3) per DIO board.

A Channel Test is a configurable, active-low, signal that evaluates the levels of all I/O Channels of a DIO board against an expected pattern and a mask. If the I/O Channel levels (that are not masked out) match the expected pattern, the Channel Test signal will transition from a high to a low and remain low until the I/O Channel levels no longer match the expected pattern. The **Channel Test 0** signal can be used as a source for the Triggers and Control Resource. All Channel Tests can be connected (provide output) to the Auxiliary Channels of a domain.

See GtDio6xSequencerSetChannelsCompareTrigger for more information.

I/O Channel Operation

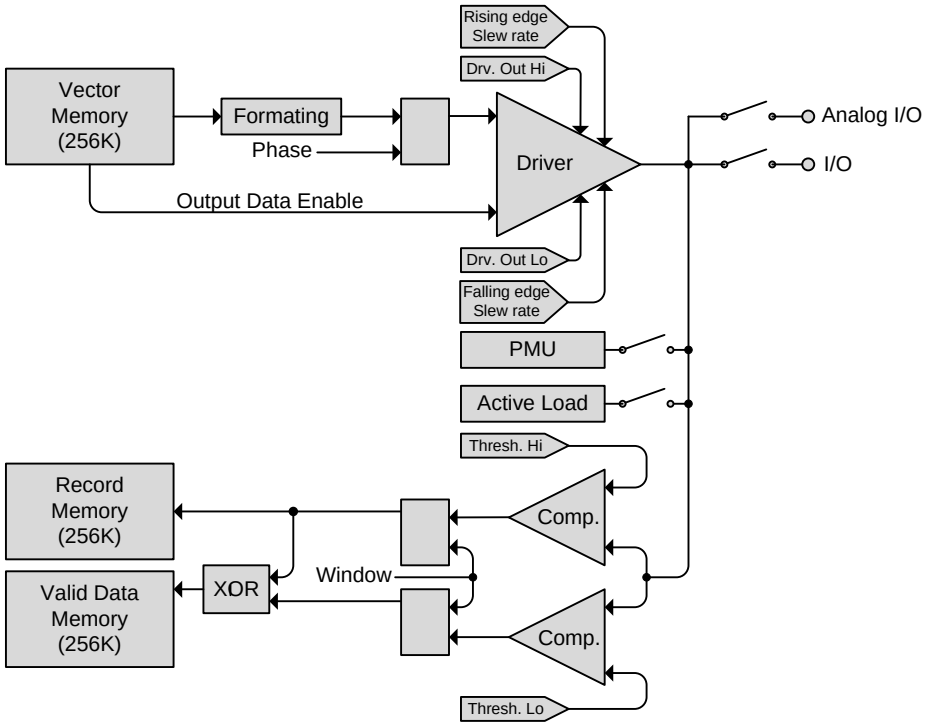


Figure 4-16: Output Data Block Diagram

Figure 4-6 is a block diagram of a single I/O pin. Up to 16 boards can be used in one domain for a maximum of 512 pins (each board containing 32 I/O pins). Output data, which is stored in the Vector memory, is outputted from the board as a function of the PHASE signal through the Driver when enabled; the encoded data (see Memory Management) enables the Driver output when the specified Vector is defined as an output Vector. The output data to the UUT will also be stored in the Record memory via the receiver pin electronics. The output data will be formatted as it was defined programmatically by the user to one of the following formats: No Return, Return to Zero, Return to One, Return to Hi-Z, Return to Complement, Surround Complement.

Each data channel's output signal has programmable Drive Out Hi and Drive Out Lo levels. The Drive Out Hi level can be set from -9 volts to +15 volts and must be greater than the output driver's Drive Out Low voltage. The Drive Out Low voltage can be set from -10 volt to +11 volts. These levels are based on a Vcc voltage of +18 volts and a Vee voltage of -14 volts. Total range for the driver and comparator voltage range is -15 V to +26 volts inclusive with a maximum span of 26 volts. Each Driver channel slew rate can be programmed, with rising and falling slew rates programmed independently.

Each Driver has output over current protection. Once an over current condition occurs, the output will be set automatically to Hi-Z impedance. The over current event can be monitored by the CPU as well as cleared under CPU control in order to re-enable the output.

The pin electronics input analog stage is comprised of a set of input pull-up and pull down resistive loads, constant current sink and source loads, and clamping (commutation) sink and source voltages. The input pull-up and the pull down resistive loads can be set to one of the following values, 240 Ohms, 290 Ohms, 1 KOhms or no load. The input resistive load is useful in applications with very low DUT output swings (where a traditional active load will not switch on and off completely or quickly) and also as a means of forcing the DUT to a known voltage when the DUT is in a Hi-Z state. In addition, the input channel programmable load can be set to have constant source and sink current loads up to 24 mA each with 0.3662 µA of resolution. The input channel's current source will force the specified constant current to be active when the input voltage is above the high voltage clamp value. The input channel's current sink forces the specified constant current to be active when the input voltage is below the low voltage clamp value.

The input signal is connected to two comparators. The threshold sense high and low voltage levels are set programmatically by the user. Both the input high and low voltage threshold values can be set from -10.0V to +11.0V. These levels are based on a Vcc voltage of +18 volts and a Vee voltage of -14 volts. The sense hi level must be higher than the input low voltage threshold and the input low voltage threshold must be lower than the input high voltage threshold. Maximum voltage range is -15 V to +26 V. Each channel's operating temperature, the Vcc / Vee voltage rails, drive high / drive low voltages, sense hi / sense lo voltages, and output current values can all be monitored and measured.

Input data is stored in the Record Memory and is stored at the rate of the Vector Clock. The Vector opcode, once decoded, (see Memory Management) enables the input when the specified step is defined as an input step.

The input data will be processed as follows:

- If input data is higher than the high voltage threshold, the input is detected as logic high. Data will be logged as logic high to the input memory and a 0 is logged to the valid data memory.
- If input data is lower than the low voltage threshold, the input is detected as a logic low. Data will be logged as a logic low to the input memory and a 0 is logged to the valid data memory.
- If input data is higher than a low voltage threshold and lower than a high voltage threshold, input is invalid. Data will be logged as a logic low to the input memory and logged as a 1 to the invalid data memory.

Note: Each channel's output and input are connected. As a result whenever a channel is defined as an output for a specified step, it will be recorded to the In Memory while running.

Programmable Input Current Load and Voltage Clamps

Each input channel's constant current source and sink load currents and its corresponding voltage clamps can be set programmatically.

The input channel's current load provides a constant current load that is active when the input voltage is above or below the high voltage or low voltage clamp values respectively. The input channel's constant current source value can be set from 0mA to 24mA with 0.3662 µA of resolution.

With independent high and low clamping (commutating) voltages, the source and sink currents each have their own threshold voltage. If the voltage on the channel input, when the load is activated, is between the two clamping voltages, the load will remain in a high impedance state (see Figure 4-18).

The input channel's source and sink constant currents can be read back and set dynamically at any time even when the DIO is in its run state.

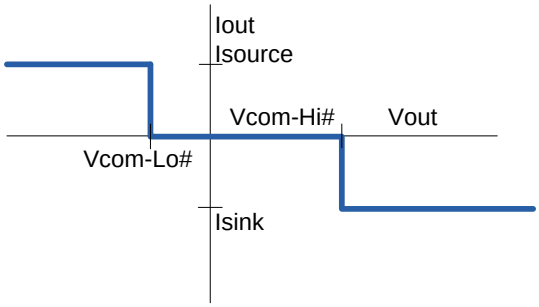


Figure 4-17: GX5960 Input Load Current Voltage Clamps

The input channel's high and low clamping (commutating) voltage values can be set from -10V to +11V when the Vcc and Vee rail voltages are set to +18 volts and -14 volts respectively. Maximum range for the Vcom voltages is -5V to +26V.

The input channel's constant current voltage clamps can be read back and set dynamically at any time even when the DIO is in its run state.

Programmable Resistive Load

Each input channel's load may be configured as a selectable resistor with pull-up and pull-down values. The resistive load is useful in applications with very low DUT output swings (where a traditional active load will not switch on and off completely or quickly) and also as a means of forcing the DUT to a known voltage when the DUT is in a Hi-Z state. When the resistive load is applied to a UUT the Hi-Z state, the DIO input maintains a low leakage current when the UUT input voltage is between the VCC and VEE supply values. The following are the resistive load options:

Pull-up	Pull-down
Open (Hi-Z)	Open (Hi-Z)
250 Ohm	250 Ohm
290 Ohm	290 Ohm
1 K Ohm	1 K Ohm

Table 4-18: Resistive Load Options

The input channel's pull-up and pull down resistive loads can be read back and set dynamically at any time even when the DIO is in its running state.

Input Threshold Voltages

Each channel has a high-speed dual voltage comparator with its own independent threshold setting. Each channel's high and low input voltage threshold comparators can be set programmatically. There are two threshold voltage level settings for each input channel: logic high level and logic low level. Each input channel can detect three voltage levels: High, low and undefined. When the input voltage is equal or greater than the threshold logic high, a logic high is recorded. When the input voltage is equal or less than the threshold logic low, a logic low is recorded. When the input voltage is between the threshold high level and the threshold low setting then the value is recorded as an in-valid logic level.

The input high and input low voltage thresholds can operate over a range from -15V to +26V with the high threshold higher than the input low voltage threshold and the low voltage threshold lower than the input high voltage threshold.

The Input channel's low and high threshold voltages can be read back and set dynamically at any time even when the DIO is in the run state.

Output Data Formatting

Each output channel's data can be formatted in five different ways:

- No Return: The output logic level stays either high or low for the duration of the clock period (default).
- Return to Zero: The signal returns to zero during the phase return edge within a clock cycle.
- Return to One: The signal returns to one during the phase return edge within a clock cycle.
- Return to Hi-Z: The signal returns to Hi-Z during the phase return edge within a clock cycle.
- Return to Complement: The Return to Complement (also called Manchester code) format ensures that each transmitted data bit has at least one transition during the phase return edge within a clock cycle. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. Return to Complement ensures frequent data transitions which are directly proportional to the clock rate which helps clock recovery. A logic low is expressed by a low-to-high transition. A logic high is expressed by high-to-low transition. The transitions which signify logic high or low occur at the midpoint of a period, the direction of the mid-bit transition indicates the data.
- Compliment Surround: Tristate driver from beginning of vector to assert time and then drive programmed level. Tristate driver at return time.
- Force Zero: Force driver to low level
- Force One: Force driver to high level
- Force Off: Force driver to Hi-Z
- Force Inverted Phase: Drive high to low at the phase assert edge and low to high at the phase return edge.
- Force Phase: Drive low to high at the phase assert edge and high to low at the phase return time.

NOTE: the specified channel data format will be applied to all the channels' vectors that are set as outputs. The inputs do not support or decode formatted data.

Output Slew Rate

Each output channel has independent adjustments for the rising and falling edge slew rates.

The driver output stage also has a programmable bias current which can be used to manage overall power consumption of the PEs, i.e. lower bias current settings can be used for lower data rate / edge rate applications. Note that the slew rate will be affected by the bias current settings. The slew rate range is programmable from 0.1 V/ns to 1.0 V/ns with a high bias current setting. The channels' slew rates can be read back and set dynamically at any time even when the DIO is in the run state.

Output Voltage Levels

Each output channel's low and high level drive voltages can be set programmatically. Each output channel's driver has two levels, low and high. The total output driver voltage swing (output driver high voltage less output driver low voltage) is limited to 25V per channel.

The output channel's driver voltages can be read back and set dynamically at any time even when the DIO is in the run state.

PMU Functionality

Each digital channel includes a parametric measurement unit (PMU) which can be used to characterize and measure a digital pin's DC characteristics. The PMU can be configured for force current, measure voltage, or force voltage, measure current. The PMU's range of operation is listed below:

Force voltage range: -10 volts to +15 volts (for Vcc = +18V and Vee = -14V)

Force curent range: +/- 30 mA FS or +/- 200 mA FS

Measure voltage range: -10 volts to +15 volts (for Vcc = +1v and Vee = -14V)

Masure curent range: +/- 30 mA FS or +/- 200 mA FS

Measurement resolution is 16 bits for both voltage and current measurement functions. Note that while each channel has a dedicated PMU, the measurement resource is shared between all 32 channels, requiring sequential measurement of each channel.

Probe

The Gx5961 has the ability to capture data from a logic probe synchronously (with the Vector Clock) using Window 3 of the currently generated timing set. The probe connection is tied to the Auxiliary Channel 0. In order to use the probe, Auxiliary Channel 0 must be connected and programmed with the appropriate ViH and ViL for the application. The VCC and VEE voltage rails must be present and the power connection should be set appropriately.

The probe can capture 34 different types of states per clock cycle and the probe memory can store up to 262144 states of information. Each state captured (one per Vector Clock cycle) provides information on what logic threshold(s) were crossed and if various types of glitching occurred. This information is encoded into an 8-bit value.

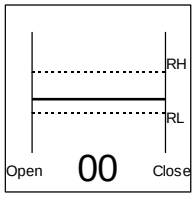
The bit descriptions for each state stored in the probe memory are:

Bit	Description
0	Good 1 level at window 3 open
1	Good 0 level at window 3 open
2	Good 1 level at window 3 close
3	Good 0 level at window 3 close
4	Positive transition at good 1 level
5	Positive transition at good 0 level
6	Negative transition at good 1 level
7	Negative transition at good 0 level

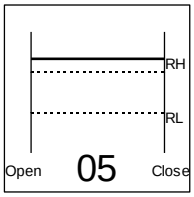
Table 4-19: Probe Memory Bit Description

See **GtDio6xProbeGetData, GtDio6xProbeSetDataMode** for more information.

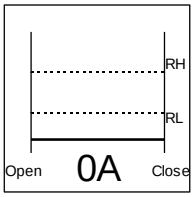
Each combination of the 8 bits describes a particular logic scenario as described in the following table (state values are in hexadecimal):



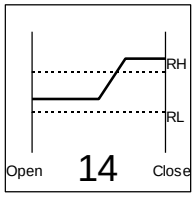
Middle – Signal remains between RL and RH.



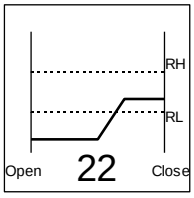
High – Signal remains above RH.



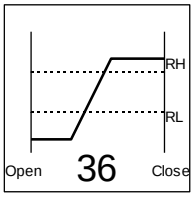
Low – Signal remains below RL.



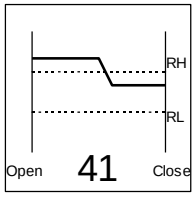
Middle High – Signal starts between RL and RH, crosses the RH once and ends above RH.



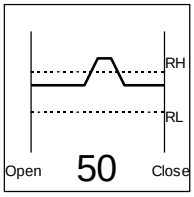
Low Middle – Signal starts below RL, crosses the RL once and ends between RL and RH.



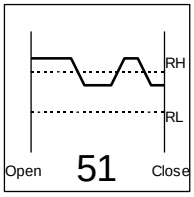
Rising Edge – Signal starts below RL and crosses the RL and RH once.



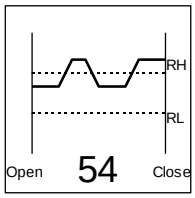
High Middle – Signal starts above RH, crosses RH once and ends between RL and RH.



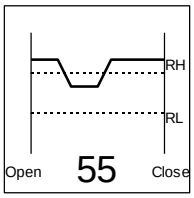
Middle Glitch - Signal starts between RL and RH, crosses the RH one or more times and ends between RL and RH.



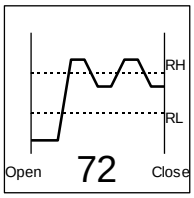
High Glitch Middle – Signal starts above RH, crosses the RH one or more times and ends between RL and RH.



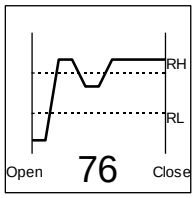
Middle Glitch High - Signal starts between RL and RH, crosses the RH one or more times and ends above RH.



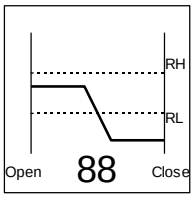
High Glitch – Signal starts above RH, crosses the RH one or more times and ends above RH.



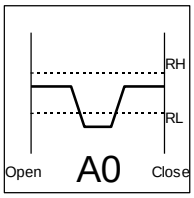
Rising Edge Glitch Middle – Signal starts below RL, crosses RL once, crosses RH one or more times and ends between RL and RH.



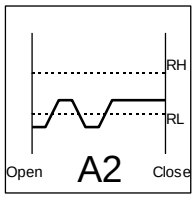
Rising Edge Glitch – Signal starts below RL, crosses RL once, crosses RH one or more times and ends above RH.



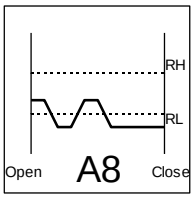
Middle Low – Signal starts between RL and RH, crosses the RL once and ends below RL.



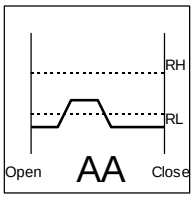
Middle Glitch - Signal starts between RL and RH, crosses the RL one or more times and ends between RL and RH.



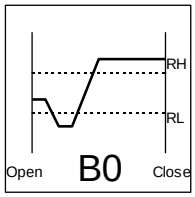
Low Glitch Middle - Signal starts below RL, crosses the RL one or more times and ends between RL and RH.



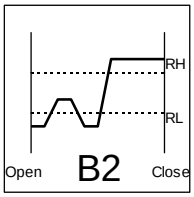
Middle Glitch Low - Signal starts between RL and RH, crosses the RL one or more times and ends below RL.



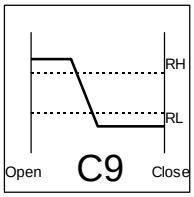
Low Glitch - Signal starts below RL, crosses the RL one or more times and ends below RL.



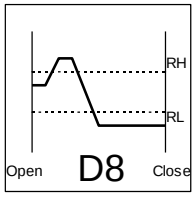
Middle Rising Edge - Signal starts between RL and RH, crosses the RL one or more times, crosses RH once and ends above RH.



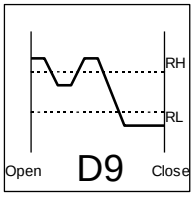
Low Glitch Rising Edge - Signal starts below RL, crosses the RL one or more times, crosses RH once and ends above RH.



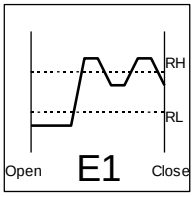
Falling Edge – Signal starts above RH and crosses the RH and RL once.



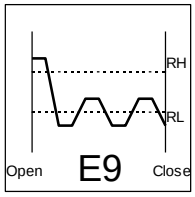
Middle Falling Edge - Signal starts between RL and RH, crosses the RH one or more times, crosses RL once and ends below RL.



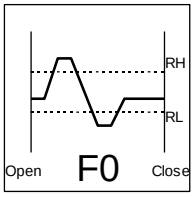
High Glitch Falling Edge - Signal starts above RH, crosses the RH one or more times, crosses RL once and ends below RL.



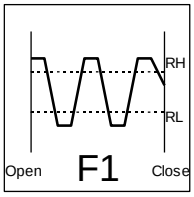
Rising Edge Glitch Middle – Signal starts below RL, crosses RL once, crosses RH one or more times and ends between RL and RH.



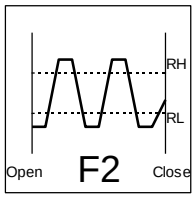
Falling Edge Glitch – Signal starts above RH, crosses RH and RL once, crosses RL one or more times and ends below RL.



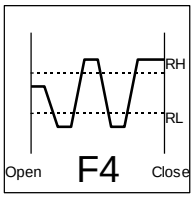
Middle Pulse Middle – Signal starts between RL and RH, crosses RH and RL two or more times and ends between RL and RH.



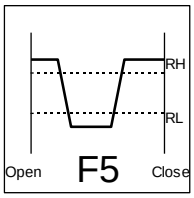
High Pulse Middle – Signal starts above RH, crosses RH and RL two or more times and ends between RL and RH.



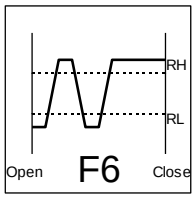
Low Pulse Middle – Signal starts below RL, crosses RL and RH two or more times and ends between RL and RH.



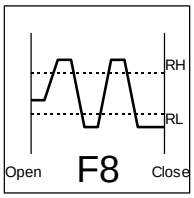
Middle Pulse High – Signal starts between RL and RH, crosses RL two or more times, RH three or more times and ends above RH.



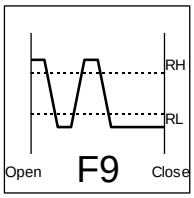
High Pulse – Signal starts above RH, crosses RH and RL two or more times and ends above RH.



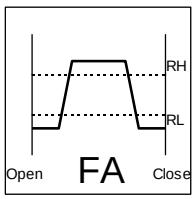
Low Pulse High – Signal starts below RL, crosses RL and RH three or more times and ends above RH.



Middle Pulse Low – Signal starts between RL and RH, crosses RL three or more times, RH two or more times and ends below RL.



High Pulse Low – Signal starts above RH, crosses RL and RH three or more times and ends below RL.



Low Pulse – Signal starts below RL, crosses RL and RH two or more times and ends below RL.

Table 4-20: Probe Memory States

Index